ARMY RESEARCH LABORATORY

A Simple Digital Method for Compensation of Baseline Drift in Low-Frequency Small-Signal Waveform Measurements

by Thomas Kottke, David M. Perry, and George M. Thomson

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Abstract

The need to measure relatively small signals mixed with drifting background levels and random noise is a common requirement in the laboratory environment. This report presents a simple device that continuously compensates for drifting baseline levels in systems where the background can be measured independently. The resulting level of automation allows the effects of random noise to be diminished through extensive signal averaging. For added flexibility, parameters such as the input voltage range and background sampling rate can be set by the user. All required hardware and software are provided and explained in detail.

Acknowledgments

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1. Introduction

In many electronic measurements, low-level broadband signals must be extracted, which are superimposed on a slowly varying background that drifts over a range many times that of the signal amplitude. The problem is compounded when the background contains higher frequency components (i.e., noise). In this report, a technique is presented that was devised at the U. S. Army Research Laboratory (ARL) to mitigate the effects of long-term baseline drift and thus allow the application of additional techniques for noise removal, such as signal averaging.

This technique is a by-product of ARL's investigations of methods for the remote detection and identification of airborne gases in the battlefield environment. One proposed method, called infrared fluorescence (IRF), uses a high-power laser to selectively excite one of an aerosol's constituent gaseous species. A telescope is then used to collect and analyze the characteristic infrared radiation emitted during that component's subsequent de-excitation processes. It is the detection of these fluorescent emissions that motivated the present work. They are not only intrinsically weak, but also superimposed on a noisy, drifting background. In the current discussion, drift and noise are distinguished by their respective nonrandom and random natures. In the IRF apparatus, drift arises from a combination of variations in the inherent thermal background radiation that permeates a room temperature environment; of changes in the properties of electronic components such as batteries, detectors, and amplifiers; and of stray electric or magnetic fields. These sources tend to be nonrepetitive and do not average out to zero over time. On the other hand, all detection systems and amplifiers are subject to a variety of random noises, such as Johnson noise, shot noise, and 1/f noise (Moore 1983). Clearly, the ability to extract the desired IR emission from the profusion of background and noise signals is both an essential requirement and a challenging task.

The ability to recover useful information from a detected signal (i.e., a mixture of a pure signal and random noise) is not a function of the absolute value of the pure signal but rather the signal-to-noise (SNR) ratio.

$$SNR = S / N \quad (1)$$

S is the amplitude of the pure signal and N is the amplitude of the random noise. The larger the SNR, the smaller the minimum detectable pure signal that can be recovered. Random noise has an equal probability of having a positive or negative sense and therefore averages out to zero over a long period of time. For a repetitive pure signal, the SNR can be increased by averaging the detected signal over multiple cycles. The improvement in the SNR with signal averaging can be expressed as:

$$SNR_{ave} = \sqrt{n} \cdot SNR_0 . \quad (2)$$

SNR_{ave} is the signal-to-noise ratio of multiple averaged signals, SNR_0 is the signal-to-noise ratio of a single detector signal measurement, and n is the number of repetitive signals that are averaged. Another signal recovery technique, lock-in amplification, may be superior to signal averaging for improving SNR when the waveform is well-defined. However, the availability of computer-assisted data acquisition systems has, in recent years, made simple signal averaging an attractive alternative to other hardware intensive methods.

As already mentioned, background drift, unlike random noise, does not have an equal probability of having a positive or negative sense. Therefore, background drift does not have to average out to zero, even over a very long period of time. As a result, signal averaging will not eliminate a drifting background from a repetitive signal. Often during signal averaging, drift deviations may accumulate to the point where they swamp the averaged signal. A differential detection technique can be utilized to eliminate the background in systems where the background can be measured separately. Figure 1 illustrates a schematic of this process. The *Signal + Background* and *Background* signals are supplied to the two inputs of a differential amplifier. The output from a differential amplifier is proportional to the difference between the two inputs. Thus, the output from the differential amplifier will be the desired pure signal with the background element removed.

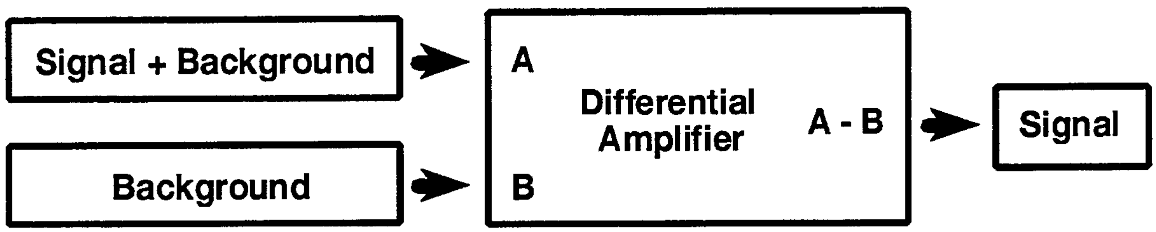

Figure 1. Schematic of the Differential Detection Process.

Clearly, the effort to recover a desired low-level signal immersed in a noisy drifting background, such as the present IR emission signal, can benefit from the application of both signal averaging and differential detection techniques—provided that the background signal can be independently measured. In the IRF scenario, the signal is the result of and temporally correlated with the pulsing of the high-power excitation laser. When the laser is off, the background signal can be measured; when the laser is on, the combined background and IR emission signal can be recorded.

With a known background signal, an external variable voltage source can be configured to mimic the measured background level. This external signal can be supplied to the background input of the differential amplifier to allow the pure IR emission signal to be separated from the background signal. An illustration of a manual method for performing this operation is presented in Figure 2. The operator, hereafter called Differential Person, observes the independently measured background signal level and adjusts the available potentiometer to a level that reproduces the current background level. This manually generated background reference signal is then subtracted from the combined IR emission and background signal via the differential amplifier.

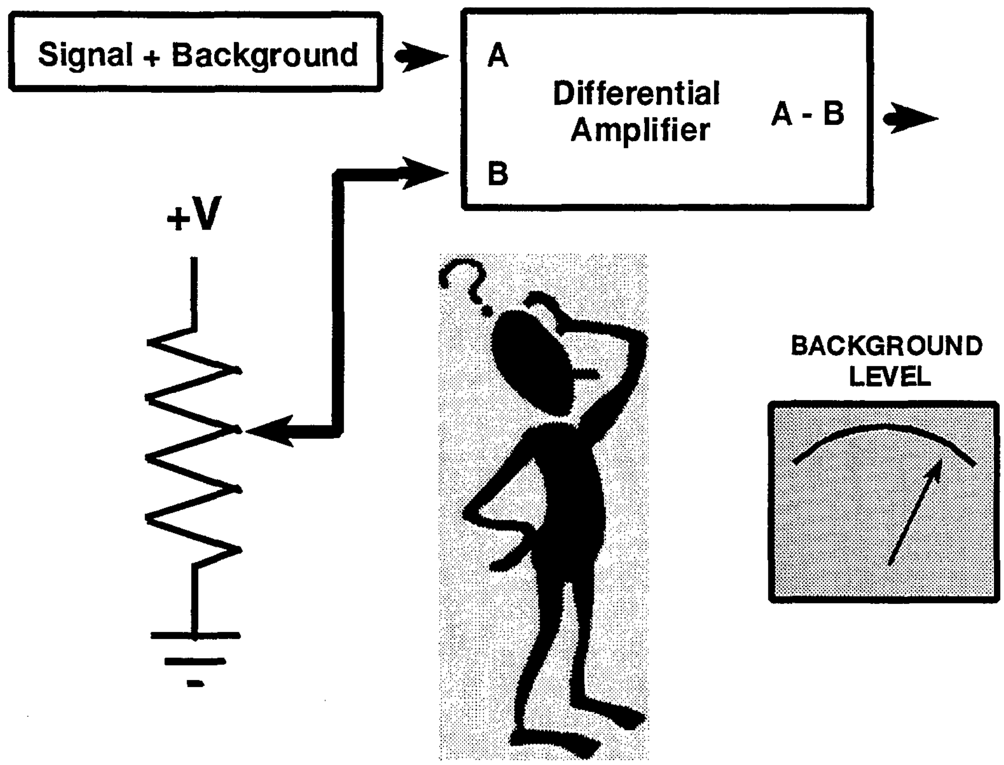

Figure 2. Manual Method for Generating External Background Signals.

Obviously, this manual method for generating the external background reference signal has a number of drawbacks. Background levels with even a moderate amount of drift may tax Differential Person's ability to manually recreate the background signal. Small signal measurements require sensitive measurement scales that span only a small fraction of the total signal's amplitudes. Under these conditions, even a minor deviation between the measured background level and the externally generated background reference signal may be sufficient to drive the differential amplifier's output signal beyond the available signal measurement range. Also, the desire to obtain a large number of repetitive measurements, so that the SNR can be reduced through averaging, may once again stress the operator's ability to consistently recreate the measured background signal level.

This report presents an automated baseline adjustment device (BAD) that can assist with the recovery of small signals that are mixed with a drifting background signal and random noise. The BAD monitors the output from the differential amplifier during periods when only the background signal is being detected. It then adjusts the potential applied to the background-only input of the differential amplifier to drive its output to a desirable baseline level. First, an overview will be presented of the hardware that performs this background subtraction process. The required electronic circuitry and its operation will then be considered in increasing detail. Included in these electronics is a controller that orchestrates the activities of the various components. The software that drives this controller will also be provided and discussed. While the apparatus described was designed for a specific application, its general operating principles, as well as many of its physical details, can be readily adapted to many signal recovery tasks.

2. Baseline Adjustment Device Embodiment

2.1 Overview. A schematic overview of the BAD hardware is illustrated in Figure 3. The ease with which this device can be implemented is due, in part, to the small number of external connections that need to be provided. A timing signal must be supplied to notify the BAD that the measurement system is currently recording only a background signal. It is during these intervals that adjustments to the baseline level are appropriate. For the IR emission measurement system this signal is synchronized with the pulsing of the high-power excitation laser. Specifically, baseline adjustments are performed while the laser is off and the detection system is recording only the ambient background level.

During the intervals that the laser is off, the BAD samples a feedback signal from the measurement system that indicates the amplitude of the present background level. In the case of the IR measurement system, this feedback is provided by the output of the differential amplifier. The actual background signal and the BAD-generated reproduction of the background level from the most recent sampling are fed into the differential amplifier's two inputs. Assuming that the background drift is not inordinately high, the differential amplifier's output can be expected to be

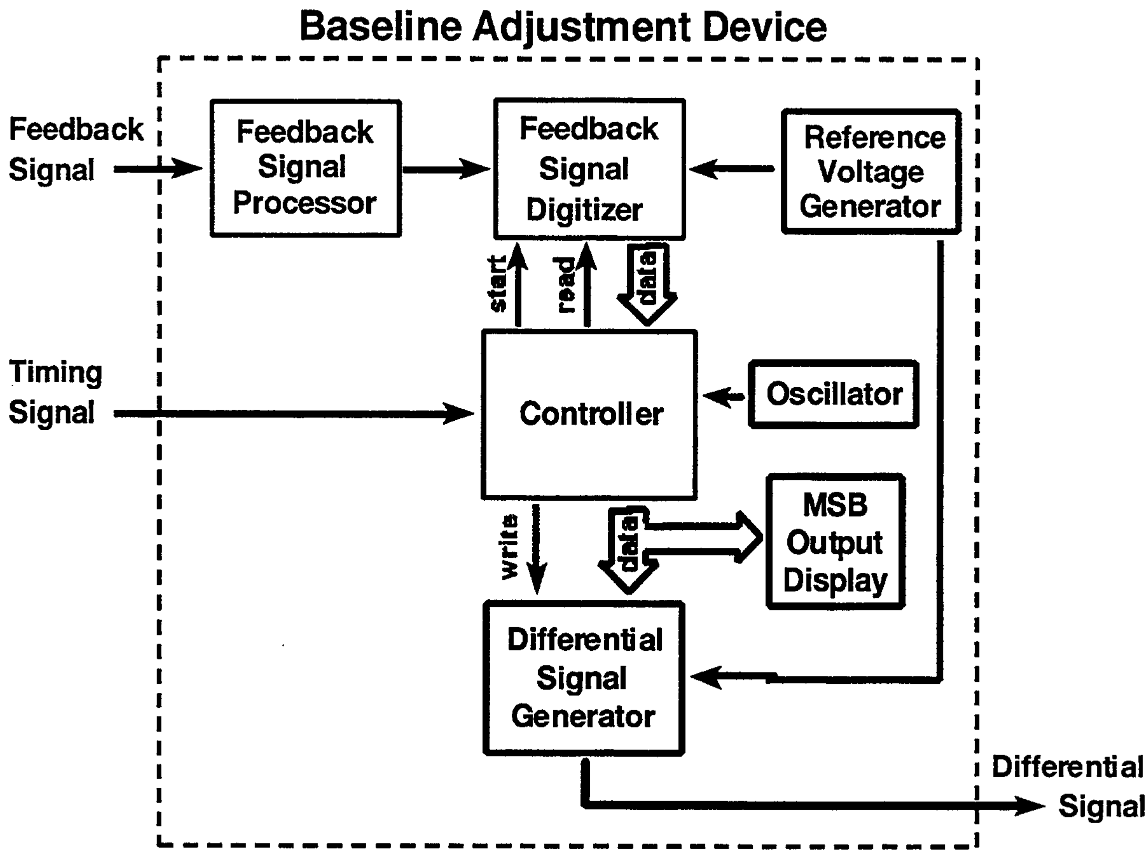

Figure 3. Schematic Overview of Baseline Adjustment Device Hardware.

near zero. This is in fact the very condition that allows small signals to be recorded on very sensitive scales. Depending on the sense in which the feedback signal deviates from the desired value, the BAD will either increase or decrease the magnitude of its output signal. This output signal provides the differential signal voltage that is looped back to the background-only input of the differential amplifier. Variations in this signal therefore alter the output from the differential amplifier. This closed-loop method has the effect of providing a signal to the background reference input of the differential amplifier that closely mimics the current background level. The BAD then resamples the feedback signal and adjusts the magnitude of the externally generated reference signal in an iterative fashion until the desired feedback signal level is obtained.

A brief overview of the electrical subsystems that make up the BAD is now provided. Input feedback signals are first scaled by a feedback signal processor. The function of this processor is to adjust the magnitude of the feedback signals to match the allowable input range of the subsequent feedback signal digitizer. This feedback signal processing is performed by an operational amplifier (op amp). The actual details of the characteristics of this op amp will depend on the constraints of the specific measurement problem. After being properly scaled, the feedback signal is digitized by an analog-to-digital convertor (ADC). This conversion from an analog to a digital signal is necessary to allow the inherently digital controller to read the current feedback signal value. The controller compares this current feedback signal level to the desired level and adjusts the value of a digital word that is output to the differential signal generator. The differential signal generator is a digital-to-analog convertor (DAC) that outputs an analog voltage that corresponds to the value of its digital input. Thus, the controller can adjust the magnitude of the analog differential signal by varying the value of the digital word that it writes to the differential signal generator.

The ADC and the DAC measure and produce analog voltages by comparing them to a reference voltage of known value. A reference voltage generator provides a constant, well-defined voltage that guarantees the accuracy of the convertor's performance. The controller's actions are paced by a crystal oscillator. Finally, the range of digital values that the controller can output to the differential signal generator is limited by the number of bits available for output. For this reason, it is desirable to operate the differential signal generator near the middle of its operating range. The most significant bits (MSB) of the digital word that the controller outputs to the differential signal generator are monitored by an MSB output display so that this condition can be maintained.

The problem described previously is also solvable by a number of analog circuits, which employ a looping process that is analogous to the method described previously. However, the utilization of digital elements of the type described in this report offer the advantages of enhanced precision, flexibility, and noise immunity. Moreover, the key components of this system are inexpensive, reliable, and widely available.

2.2 Electronic Details. The electronic circuitry and its operation are now presented in detail. A schematic diagram of this circuitry is illustrated in Figure 4. The two required inputs to the BAD are shown in the upper left-hand corner of this figure. For the IR emission measurements, the feedback signal is provided by the output from the differential amplifier, which is amplified and buffered through the vertical signal out port of a digital processing oscilloscope. This buffered output has a maximum range of ±2 volts. As configured, the ADC0805 ADC that is used to digitize the feedback signal can convert analog signals over the range from 0 to 5 volts (National Semiconductor Company 1993). The feedback signal is matched to the measurement range of the ADC by the feedback signal processing circuitry consisting of the op amp IC1-A and the resistance dividing network of R8 and R9. The LM324 op amp is configured as a noninverting amplifier with a gain of 2.5. Thus, this op amp converts the ±2-volt feedback signal to a ±5-volt signal. This amplified signal is divided by the resistance network of R8 and R9 that is referenced to the +5-volt potential of V5REF. The function of this resistor network is to convert the bipolar ±5-volt output from the op amp to a 0–5-volt signal that matches the measurement range of the ADC.

The external timing signal is routed to the RA3 input line of the PIC16C55 controller. When the controller determines that the timing signal indicates that background adjustment is appropriate, the controller initiates an ADC by sending a negative pulse from its RA2 output to the WR bar input of the ADC0805. After waiting a period of time that exceeds the ADC's conversion time, the controller instructs the ADC to output the new conversion value on its DB# output lines by pulling its RD bar input low via output line RA1. The controller then reads in this value through its RB# inputs. The 8-bit size of this digital word and the 5-volt measurement range of the ADC offer conversion resolutions of approximately 19 mV.

The PIC16C55 controller compares the new ADC conversion value to a preprogrammed target value and determines the sense of the deviation. Depending on whether the conversion value is too high or too low, the controller will decrease or increase the value of the digital word

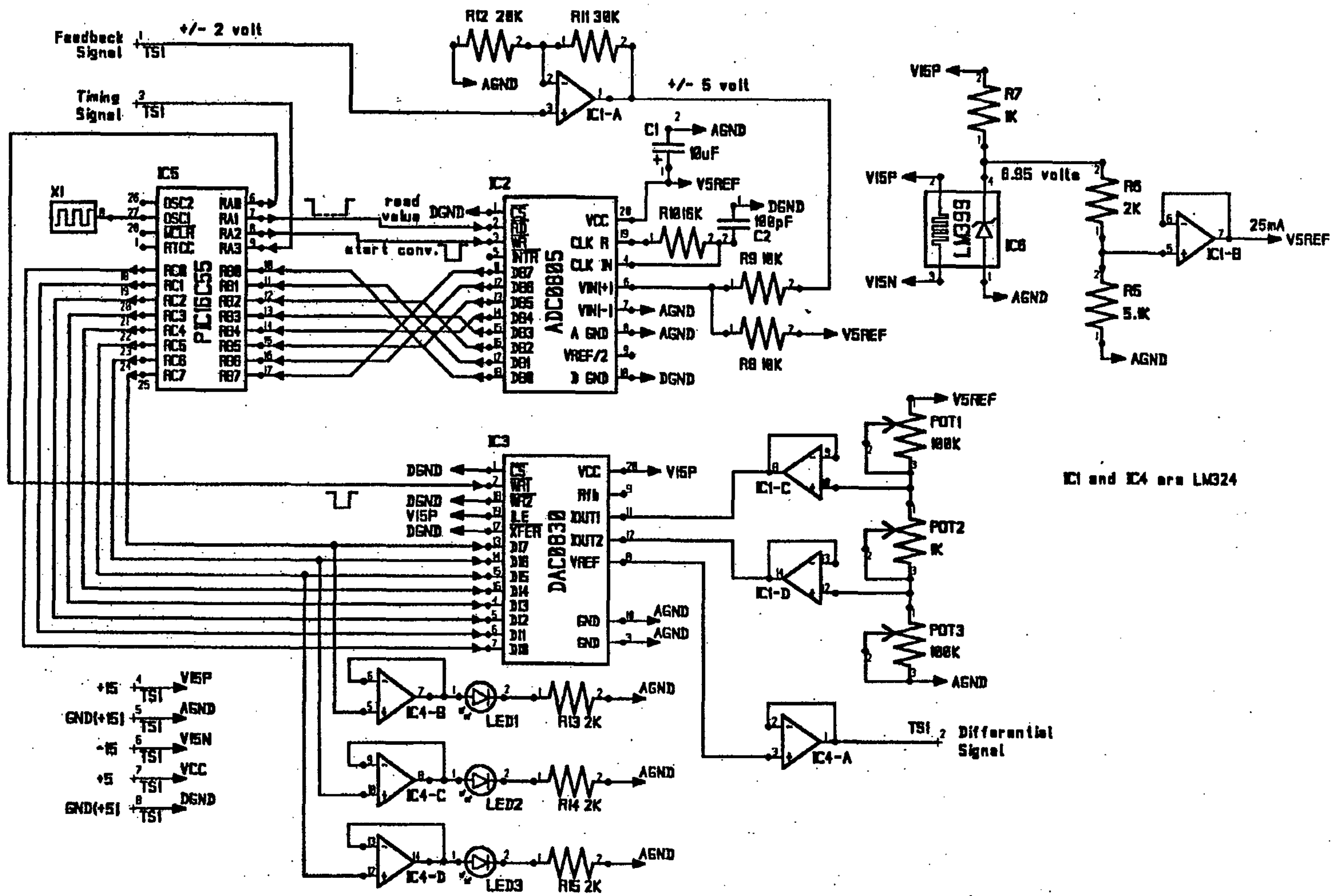

Figure 4. Schematic Diagram of Baseline Adjustment Device Electronics.

that it writes to the DI# inputs of the DAC0830 DAC via its RC# output lines. The controller forces the DAC to read in this new value by sending a low pulse from its RA0 output to the DAC's WR1 bar input.

The DAC0830 DAC uses an internal network of resistors to generate an output voltage that has a value between the potential supplied to input IOUT2 and the potential supplied at IOUT1. Specifically, the output voltage at VREF will be:

$$V_{VREF} = V_{IOUT2} + (D/256) \times (V_{IOUT1} - V_{IOUT2}). \quad (3)$$

V_{VREF} is the DAC output voltage at VREF, V_{IOUT2} is the potential supplied to input IOUT2, V_{IOUT1} is the potential supplied to input IOUT1, and D is the value of the digital word ($0 \leq D \leq 255$) supplied to the input's DI#. This ability to determine the range and span of DAC output values allows the required precision of the differential signal to be achieved. In combination, the potentiometers POT1 and POT3 determine the range of analog voltages that the DAC can produce. The magnitude of the setting of POT2, relative to the settings of POT1 and POT3, determines the span of the DAC's output range. By setting POT2 arbitrarily small, the output precision of the DAC can be made arbitrarily high over a very small range of voltages. Op amps IC1-C and IC1-D are used to buffer the input voltages from the potentiometer network to the DAC IOUT1 and IOUT2 inputs, while op amp IC4-A buffers the DAC's output voltage.

The BAD's ability to compensate for drifting background levels is maximized when the DAC is supplying a voltage that is near the middle of its range of output voltages. This condition is monitored by noting the value of the MSBs. The data lines of the DAC's three MSBs are buffered by op amps IC4-B, IC4-C, and IC4-D, and the corresponding data is displayed by LED1, LED2, and LED3. When operating, the potentiometer network is adjusted so that either LED1 is on while LED2 and LED3 are off or LED1 is off while LED2 and LED3 are on. Either of these conditions denote that the DAC is operating near the middle of its allowed range of output voltages.

A number of supply voltages must be provided to this electronic circuitry. For instrumentation that incorporates both analog and digital components, it is generally desirable to isolate the corresponding power supplies. This practice shields the analog components from the spikes that are commonly found on digital power lines. The digital power requirements are fulfilled by the 5-volt potential supplied across VCC and DGND. Analog power is provided via the +15-volt potential between V15P and AGND, and the −15-volt potential across V15N and AGND. These ±15-volt potentials are supplied directly to the op amps and the DAC. A +5-volt potential is also derived from the ±15-volt supply by an LM399 precision reference (National Semiconductor Company 1988). This monolithic device incorporates an active zener that is temperature stabilized by a heater to provide a stable, low-power reference voltage. An op amp scales this reference voltage to the required 5-volt potential and increases the available drive current to greater than 25 mA. This precision 5-volt potential between V5REF and AGND powers the potentiometer network and the analog portion of the ADC.

3. Baseline Adjustment Device Software

The internal processes of the BAD are orchestrated by a PIC16C55 controller. Specifically, the controller synchronizes the BAD's operation with the background-only phase of the measurement system, initiates the ADCs of the feedback signal, and adjusts the magnitude of the differential signal in an appropriate manner. The controller performs these operations by repeatedly executing the instructions contained in its erasable read-only memory (EPROM). A flowchart of this software is presented in Figure 5. For clarity, the macros that perform described functions are enclosed in square brackets in this figure. A listing of this code is presented in the Appendix.

When the PIC16C55 controller is powered up, a number of initializing procedures are executed. Upon power up, the input/output (I/O) pins default to a high-impedence input state. The macro SetTRIS defines the appropriate status of the I/O pins as either input or output. Even though the real-time clock/counter (RTCC) and watch-dog timer (WDT) capabilities of the PIC16C55 are not utilized in this application, the SetOPTION macro is used to define the associated option

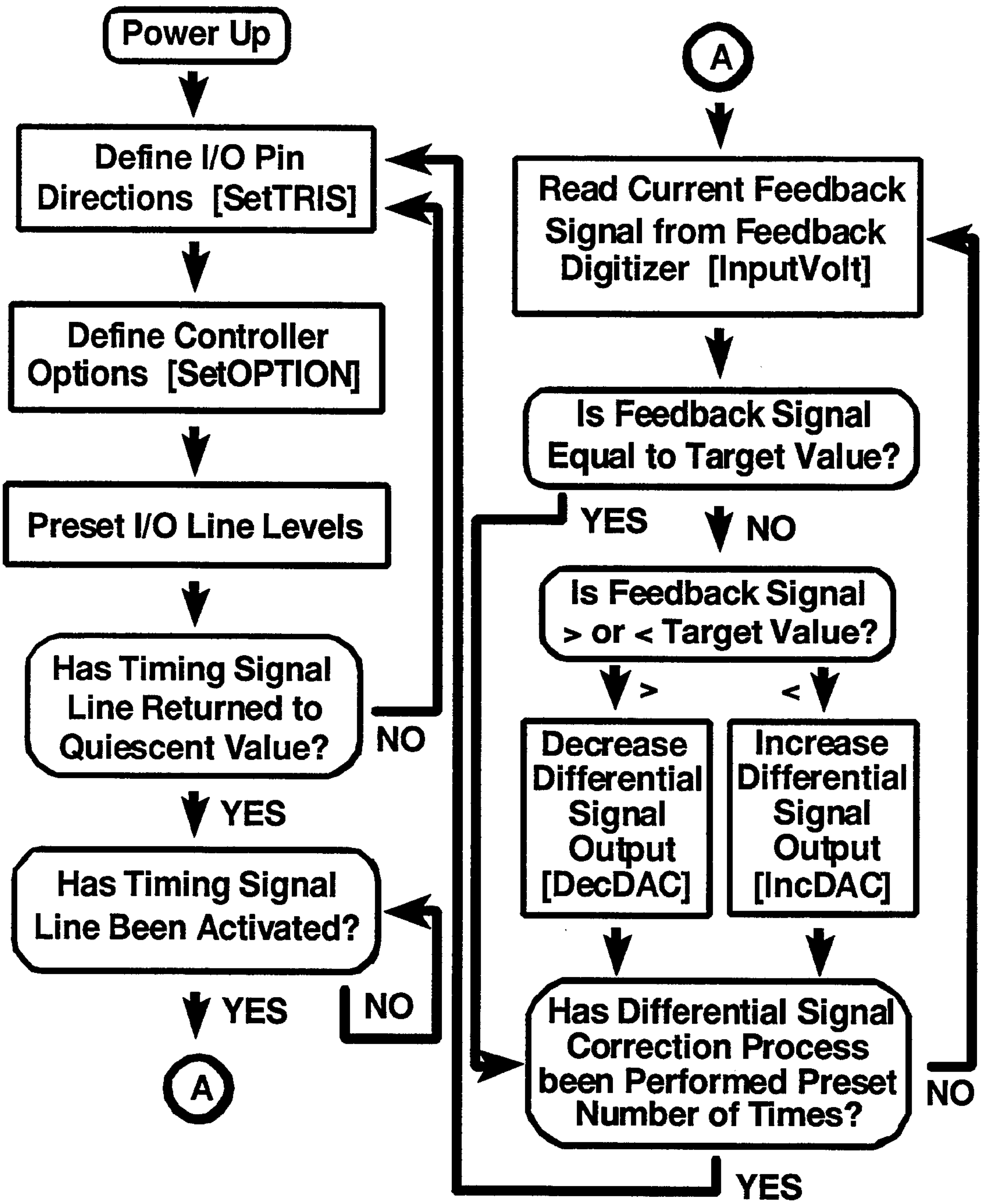

Figure 5. Flowchart of PIC16C55 Controller Software.

register to convenient, benign values. The I/O pins that were defined to be outputs are then set to an initial state that is compatible with the connected components. These initializing procedures are actually executed on a regular basis to avoid potential problems resulting from the corruption of register contents, which can occur in electrically noisy environments (Microchip Technology Inc. 1992).

Once the initiation process is completed, the controller monitors the timing signal input line to determine when baseline adjustment is appropriate. After the measurement system has entered a background-only phase, the controller initiates an ADC and reads in the current value of the feedback signal. If this feedback signal matches the preprogrammed target value, then background adjustment is not required. If the feedback signal is found to deviate from the target value, the controller then determines the sense of the deviation and increases or decreases the magnitude of the differential signal as appropriate. This differential signal adjustment process is repeated a preset number of times that depend on the time interval available and the estimated maximum background drift. The initialization routine is then reentered, and the entire process is repeated as a free running loop.

4. A Performance Example

Figure 6 illustrates an example of the BAD's performance. The upper oscilloscope trace displays a collection of repetitive, narrow rectangular pulses superimposed on a relatively low-frequency ramped-sawtooth waveform. For the purposes of this example, the narrow pulses represent the desired signal that is to be recovered and the broad sawtooth mimics a drifting background that is to be eliminated. The middle trace shows the independent measurement of this background signal as it is fed into the feedback signal input of the BAD. An appropriate timing signal is supplied to the BAD's timing input that triggers the BAD to update the magnitude of its differential output signal every 20 mS. This differential signal is routed to one input of a differential amplifier while the signal shown in the upper trace is routed to the other input. The output from the differential amplifier, which is the difference between its two inputs, is shown by the bottom trace. The low-frequency sawtooth background signal is effectively

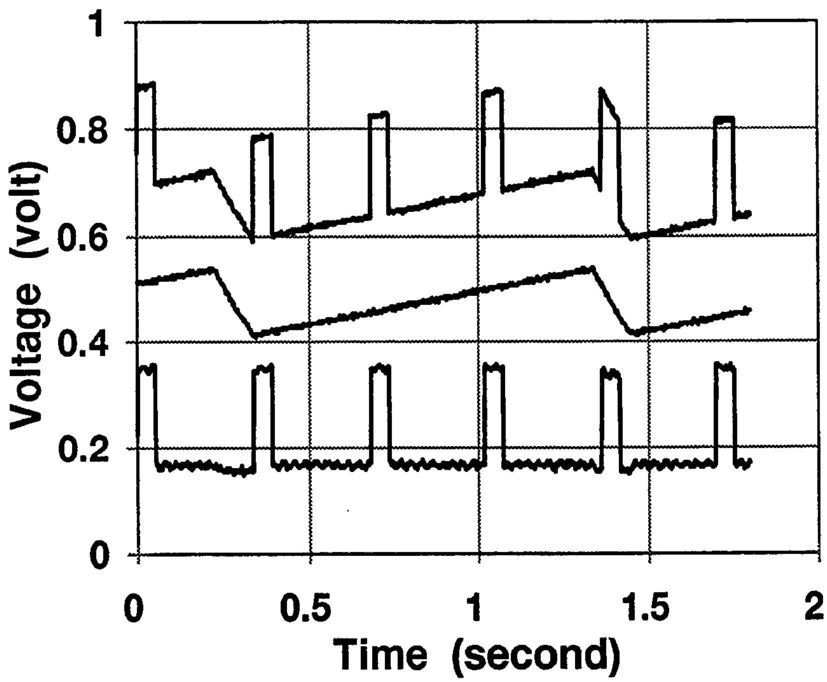

Figure 6. Example of Baseline Adjustment Device Performance.

eliminated. Signal averaging techniques could now be applied to this recovered signal to eliminate the presence of random noise.

5. Conclusions

An automated baseline adjustment device has been presented that can simplify the measurement of small signals that are combined with a drifting background signal and random noise. Although developed to assist with the measurement of IR emissions from gaseous media, this system can be applied generally to systems that offer an independent measurement of the background level. The required hardware has been presented in increasing complexity beginning with an overview of the instrument's functions and progressing through a complete description of the electronic circuitry and its logic. Similarly, the software that drives the embedded controller is presented as a flowchart, explained in detail, and listed in the Appendix.

6. References

Microchip Technology Inc. *Microchip Data Book.* Second edition, Chandler, AZ, 1992.

Moore, J. H., C. C. Davis, and M. A. Coplan. *Building Scientific Apparatus.* Reading, MA: Addison-Wesley Publishing Co., Inc., 1983.

National Semiconductor Company. *Linear Databook 2.* Santa Clara, CA, 1988 edition.

National Semiconductor Company. *Data Acquisition Databook.* Santa Clara, CA, 1993 edition.

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Appendix:

PIC16C55 Controller Software Listing

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```
; IR FLUORESCENCE BASELINE ADJUSTMENT DRIVER
; PROGRAM FOR PIC16C55 MICROCONTROLLER

; VERSION 3.0  JULY 1997
; WRITTEN FOR ASSEMBLY BY MICROCHIP TECHNOLOGY MPALC
; MACRO ASSEMBLER.

; IF YOU HAVE ANY QUESTIONS ABOUT THIS SOFTWARE CONTACT:
;    Dr. Thomas W. Kottke
;    AMSRL-WM-WD
;    Army Research Laboratory
;    Aberdeen Proving Ground, MD 21005
;    tel: (410) 278-2557
;    fax: (410) 278-9969
;    e-mail: kottke@arl.army.mil

;*********************** EQUATE VALUES ***********************

;------------------- CONSTANT DEFINITIONS --------------------
W           EQU     0x00            ;direct action result
                                    ; to W
F           EQU     0x01            ;direct action result
                                    ; to F##
Target      EQU     b'01100000'     ;target differential
                                    ; op amp output
NumCor      EQU     b'00011000'     ;# correction steps

;---------------------- BIT DEFINITIONS ----------------------
CarryBit    EQU     0x00            ;carr flag of
                    ; Status regist
ZeroBit     EQU     0x02            ;zero flag of Status
                                    ; register
DACWrite    EQU     0x00            ;bit 0 of HandShake
ADCRead     EQU     0x01            ;bit 1 of HandShake
ADCWrite    EQU     0x02            ;bit 2 of HandShake
Trigger     EQU     0x03            ;bit 3 of HandShake

;------------------- REGISTER DEFINITIONS --------------------
Status      EQU     0x03            ;status register, R3
HandShake   EQU     0x05            ;handshaking reg, R5
ADCInput    EQU     0x06            ;ADC input reg,   R6
DACOutput   EQU     0x07            ;DAC output reg,  R7
Looper      EQU     0x08            ;interval delay
                                    ; counter reg,    R8
ADCValue    EQU     0x09            ;ADC value reg,   R9
DACValue    EQU     0x0A            ;DAC value reg,   R10
```

```
LoopCor     EQU         0x0B                ;correction
                                            ; counter reg.    R11
PrevVal     EQU         0x0C                ;previous value   R12

;********************** MACRO DIRECTORY **********************
;SetTRIS    defines I/O pin directions
;SetOPTION  set prescalar options
;Standby    place 16C55 in standby mode
;InputVolt  reads in voltage via ADC
;OutputVolt sources voltage via DAC

;********************** MACRO LISTINGS ***********************
SetTRIS     MACRO                           ;MACRO to set I/O
            ; directions
                                            ;0=output  1=input
            MOVLW       b'1000'             ;define HandShake
                                            ; template
            TRIS        HandShake           ;load R5 TRIS reg

            MOVLW       b'11111111'         ;def ADCInput
                                            ; template
            TRIS        ADCInput            ;load R6 TRIS reg

            MOVLW       b'00000000'         ;def DACOutput
                                            ; template
            TRIS        DACOutput           ;load R7 TRIS reg

            ENDM                            ;end of MACRO

;--------------------------------------------------------------
SetOPTION   MACRO                           ;MACRO to set
                                            ; prescalar options
            MOVLW       b'00111111'         ;def OPTION template
            OPTION                          ;load OPTION register

            ENDM                            ;end of MACRO

;--------------------------------------------------------------
Standby     MACRO                           ;MACRO to place 16C55
                                            ; in standby mode
            SetTRIS                         ;set I/O directions
            SetOPTION                       ;set prescalar
                        ; options
            BSF         HandShake,DACWrite;set DACWrite high
            BSF         HandShake,ADCRead ;set ADCRead high
```

```
            BSF         HandShake,ADCWrite;set ADCWrite
                        ; high
            CLRWDT                        ;clear watch dog
            ; timer

            ENDM                          ;end of MACRO

;-------------------------------------------------------------
InputVolt   MACRO                         ;MACRO to read in a
                                          ;voltage from ADC
            LOCAL       InputVolt1        ;define location
            LOCAL       InputVolt2        ;define location
            BCF         HandShake,ADCWrite;pull ADCWrite low
            MOVLW       b'00010000'       ;load W with value
            MOVWF       Looper            ;transfer W to Looper
InputVolt1  DECFSZ      Looper,F          ;decr Looper, =0 ?
            GOTO        InputVolt1        ;(no) go to In..Volt1
            BSF         HandShake,ADCWrite;(yes)pull ADCWrite
                                          ; high
            MOVLW       b'11111111'       ;load W with value
            MOVWF       Looper            ;transfer W to Looper
InputVolt2 DECFSZ       Looper,F          ;decr Looper, =0 ?
            GOTO        InputVolt2        ;(no) go to In..Volt2
            BCF         HandShake,ADCRead ;(yes) pull ADCRead
                                          ; low
            NOP                           ;settling delay
            NOP
            NOP
            MOVF        ADCInput,W        ;move ADCInput to W
            MOVWF       ADCValue          ;move W to ADCValue
            BSF         HandShake,ADCRead ;pull ADCRead high

            ENDM                          ;end of MACRO

;-------------------------------------------------------------
OutputVolt MACRO                          ;MACRO to source a
                                          ;voltage through DAC
            LOCAL       OutVolt1          ;define location
            MOVF        DACValue,W        ;move DACValue to W
            MOVWF       DACOutput         ;move W to DACOutput
            BCF         HandShake,DACWrite;pull DACWrite low
            MOVLW       b'00010000'       ;load W with value
            MOVWF       Looper            ;move W to Looper
OutVolt1    DECFSZ      Looper,F          ;decr Looper, =0 ?
            GOTO        OutVolt1          ;(no) go to OutVolt1
            BSF         HandShake,DACWrite;pull DACWrite high
```

```
            ENDM                                    ;end of MACRO

;------------------------------------------------------------

;*********************** SOURCE CODE ***********************

NotReady    Standby                                 ;MACRO
            BTFSC       HandShake,Trigger           ;trigger line clear?
            GOTO        NotReady                    ;(no) go to NotReady
Ready       BTFSS       HandShake, Trigger          ;(yes) trig line set?
            GOTO        Ready                       ;(no) go to Ready
            MOVLW       NumCor                      ;(yes) load W
            MOVWF       LoopCor                     ;move W to Looper
Correct     InputVolt                               ;MACRO
            MOVLW       Target                      ;load W with Target
                                                    ; value
            SUBWF       ADCValue,W                  ;sub W from ADCValue
            BTFSC       Status,ZeroBit              ;result=0 ?
            GOTO        Check                       ;(yes) go to Check

            BTFSS       Status,CarryBit             ;(no) result<0 ?
            GOTO        IncDAC                      ;(yes) go to IncDAC
            GOTO        DecDAC                      ;(no) go to DecDAC
IncDAC      MOVF        DACValue,W                  ;move DACValue to W
            MOVWF       PrevVal                     ;move W to PrevValue
            INCF        DACValue,F                  ;increment DACValue
            BTFSC       Status,ZeroBit              ;DACValue=0 ?
            GOTO        DACOver                     ;(yes) go to DACOver
            GOTO        DACNoOver                   ;(no) go to DACNoOver
DACOver     MOVLW       b'11111111'                 ;load W with 255
            MOVWF       DACValue                    ;move W to DACValue
DACNoOver   OutputVolt                              ;MACRO
            GOTO        Check                       ;jump

DecDAC      MOVF        DACValue,W                  ;move DACValue to W
            MOVWF       PrevVal                     ;move W to PrevValue
            DECF        DACValue,F                  ;decrement DACValue
            MOVLW       b'11111111'                 ;load W with 255
            SUBWF       DACValue,W                  ;sub W from DACValue
            BTFSC       Status,ZeroBit              ;DACValue=255 ?
            GOTO        DACUnder                    ;(yes) go to DACUnder
            GOTO        DACNoUnder                  ;(no) goto DACNoUnder
DACUnder    CLRF        DACValue                    ;set DACValue=0
DACNoUnder  OutputVolt                              ;MACRO

Check       DECFSZ      LoopCor                     ;Dec LoopCor, =0 ???
```

```
GOTO        Correct           ;(no) go to Correct

MOVF        PrevVal,W         ;(yes) move PrevVal
                              ; to W
SUBWF       DACValue,W        ;subt W from DACVal
BTFSS       Status,CarryBit   ;is carry bit set ??
GOTO        NotReady          ;(no) go to NotReady
MOVF        PrevVal,W         ;(yes) move PrevVal
            ; to W
MOVWF       DACValue          ;move W to DACValue
OutputVolt                    ;MACRO
GOTO        NotReady          ;go to NotReady
END                           ;end of code
```

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The need to measure relatively small signals mixed with drifting background levels and random noise is a common requirement in the laboratory environment. This report presents a simple device that continuously compensates for drifting baseline levels in systems where the background can be measured independently. The resulting level of automation allows the effects of random noise to be diminished through extensive signal averaging. For added flexibility, parameters such as the input voltage range and background sampling rate can be set by the user. All required hardware and software are provided and explained in detail.

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