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Ka-Band Instrumentation Radar: State Machine Design Approach and Implementation

by Francois J. Koenig

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Sensors and Electron Devices Directorate, ARL

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14. ABSTRACT We present in this report a new state machine board to control the operation of an Army Research Laboratory (ARL) Ka-Band instrumentation radar. The board provides the necessary timing signals to the RF section to control transmit pulse width, receiver protection switches, and the polarization switch. It also provides the IF section with an IF switch control, a video bias control and up to 8 bits of phase control. It provides the frequency synthesizer board with 15-bit frequency data and a signal to strobe it into registers. Finally, it provides the data acquisition system with a signal to begin sampling incoming data. Resolution of the timing signals has improved from 100 ns for the previous state machine board to 25 ns for the new board. The more critical signals can be fine tuned to a few nanoseconds with on-board delay chips. Perhaps, most significant of all is that unlike the previous design, this state machine can be reconfigured during operation, allowing timing adjustments, adjustment to the number of frequencies and step size, changes to starting phase and phase increment. It will eliminate significant down-time for reconfiguration while providing a flexible interface for user control.					
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1. Introduction

A new state machine board has been designed and built for the Army Research Laboratory Ka-Band instrumentation radar. The state machine is needed to provide timing signals, shown in figure 1, for step-frequency operation in a precise sequence and repeated at a defined interval. It controls the transmit pulse width, receiver protection switches, and the polarization switch in the RF section. It provides the IF section with an IF switch control, a video bias control and up to 8 bits of phase control. It also provides the frequency synthesizer board with 15-bit frequency data and a signal to strobe it into registers. Finally, it provides the Analog to Digital (A/D) converters of the data acquisition system with a clock signal to sample incoming data.

The new design incorporates Very High Speed Integrated Circuit Hardware Description Language (VHDL) code residing in a Field Programmable Gate Array (FPGA) for precision real time operation and a single board computer controlling a graphical user interface (GUI) for changing high-resolution timing, number of frequencies, pulses per polarization and phase values. Additional on-board hardware provides programmable attenuator control, a 4x Phase Lock Loop (PLL) clock multiplier and fine resolution delay timing for critical signals.

The previous version of the state machine provided the required timing signals with a resolution of 100 ns and burned into Electrically Programmable Read Only Memory (EPROM). A user created a 'C' program to define each timing signal and its corresponding digital state for each 100 ns time interval for the duration of one frequency step interval. (It is assumed that the states repeat for each step frequency.) Then, the program would translate the states into a time-ordered hex dump output to be loaded into the EPROM. Any adjustment in pulse repetition interval (PRI), number of pulses per frequency, number of step frequencies, frequency increment, or phase increment required reprogramming the EPROMs, subject to user programming error, and significant down-time.

The new state machine provides timing signals to a resolution of 25 ns, with critical signals to a resolution of a few nanoseconds. The medium resolution timing is completely controlled by a GUI tied to a single board computer communicating with a PC. The fine resolution is currently controlled by dip switches.

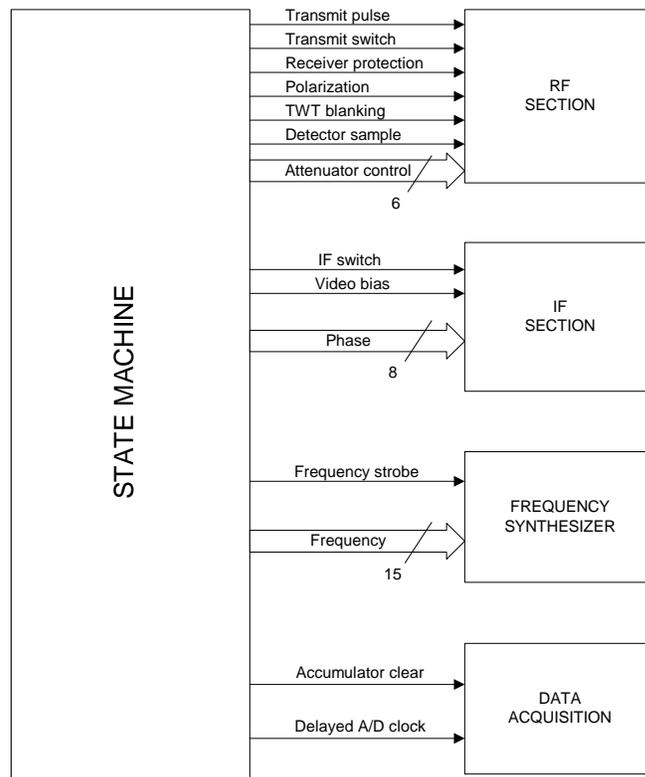


Figure 1. Timing signals needed from the state machine for radar operation.

2. Background

A Ka-Band Monopulse, Fully Polarimeter, Coherent, Instrumentation grade radar was designed by the Millimeter Wave Branch. The purpose was to support the data collection requirements necessary to generate high resolution, Inverse Synthetic Aperture Radar (ISAR) images. Originally, the radar system was designed for outdoor turntable measurements where the radar is positioned on a tower and illuminates the target on the rotating turntable. At prescribed angular rotation positions of the turntable, a burst mode occurs whereby a repetitive series of measurements are conducted. To minimize the collection time, the Pulse Repetition Frequency (PRF) was chosen to be 1 MHz with a desired full rotation of the turntable to be achieved in 10 minutes. The radar was designed to be a stepped frequency, pulsed system. To achieve high resolution range measurements, a large bandwidth of the transmit signal is required. A sequence of pulses is transmitted such that each pulse has a slight difference in the transmitted frequency. With the resulting wide bandwidth span coverage of the transmit frequencies and post processing,

an effective high resolution is obtained. To improve on the quality of the data, there are a series of functions/options that have been incorporated into the radar operation. These deal with the following: S/N improvements through integration, correction of errors associated with the Inphase/Quadature (I/Q) mixer, bias input to the A/D converter and optimally setting the sampling time for the A/D. Integration or summation of pulse response is achieved by repeating the measurement for a pre-selected number of pulses. The I/Q mixers have errors in gain and phase imbalances along with a DC offset. The effects of these errors are reduced through a technique of phase modulating the transmitting signal through known phase shifts to achieve a full phase shift through the series of pulses and post processing of the data to remove the measured errors. At the input to each A/D converter, there is a DC nulling circuitry that samples the input and nulls the DC output value to zero in order to center the signal such that the A/D convert limits equally on positive and negative signal levels, thereby obtaining the use of the full dynamic range of the A/D. A very fine time resolution step is necessary on the A/D timing in order to position the A/D converter sample to align to the proper target range. The salient features of the Ka radar are summarized in Appendix A. Since the original design, the radar system has been used to acquire data in an Anechoic chamber which required a shorter transmit pulse width to better match the limited physical range limitation as a result of the chamber walls.

3. Configuration

The major sections of the state machine configuration, shown in figure 2, consists of a 4x Phase Lock Loop Clock, a Xilinx FPGA, a Rabbit single board computer and the Logic and Fine Timing Adjustment circuit. These sections are detailed below.

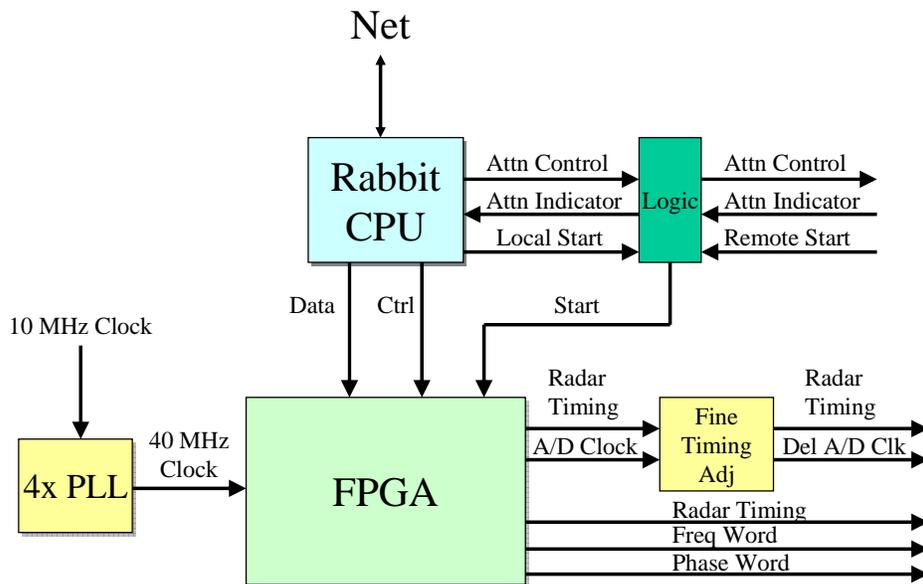


Figure 2. State Machine Configuration.

3.1 4x Phase Lock Loop Clock

It was desirable to use a finer time resolution in the FPGA than the 100 ns which could be obtained from the 10 MHz system clock. Forty MHz was selected for the FPGA clock providing a time resolution of 25 ns. To produce the 40 MHz clock, a 4x circuit was needed. Ordinarily, two Delay Lock Loop (DLL) modules within the FPGA could be used for quadrupling the input clock speed. However, the minimum lockable input clock speed for the DLL is 25 MHz. Thus, we had to create a 4x clock by another means. A Phase Lock Loop (PLL) chip was selected for the operation. Such a chip, Pericom P16C918, is available on the Associated Professional Systems (APS) – V240 development board being used. The chip has 2 multiplier select lines allowing 2x, 4x, 5x, or 7x operation. The on-board Complex Programmable Logic Device (CPLD) must be programmed to enable the chip and select the desired multiplier. Hence, the 10 MHz system clock, developed from a stable crystal oscillator, is provided to the PLL for a 4x multiplication to 40 MHz.

3.2 FPGA

The FPGA used in this application is a Xilinx Virtex XCV400, containing about 468 thousand system gates. It is small by today's standard of multi-million gate chips but it has more than enough capacity to program the required timing signals and is rich in I/O lines. The FPGA resides on the APS-V240 board and receives its programming on power up from an on-board serial EPROM. The EPROM is programmed through the JTAG ports with Xilinx software such as Foundation, running on a PC. It is within the FPGA that two main processes run, one process to receive commands and timing configuration data from the Rabbit single board computer, and the other process to generate all the output timing signals by cycling through a state machine. Analysis of the radar operation and the previous state machine board showed that we can decompose the timing requirements into a four-state, state machine. The four operating states of the state machine, Reset, Idle, State1, and State2 will be described in detail in the Timing and Control section. There are about a dozen output timing signals provided for the radar operation, in addition to a 15 bit frequency word sent to the frequency synthesizer, and an 8-bit phase word sent to the phase modulator. The FPGA VHDL design also includes a divide-by-4 output clock which synchronizes the external A/D operation with the start of the state machine's active states after receiving an input start signal. Given a 40 MHz input clock, it will produce a 10 MHz output clock. This output clock can be further adjusted in delay in 10 ns increments by a 4-bit programmable delay chip controlled by the on-board Rabbit computer. These signals will also be covered in the Timing and Control section.

3.3 Rabbit CPU

The single board computer is a low cost RCM3200 RabbitCore development board from Rabbit Semiconductor. It provides up to 52 parallel I/O lines as well as an ethernet port. A special serial interface allows downloading a 'C' program from a PC, compiling and executing it. The initial simple user interface was written in Dynamic 'C' and programmed into the Rabbit. It provided an

ASCII display on the PC for configuring each radar timing parameter which is to be generated in the FPGA. Each configuration is downloaded to the FPGA as one or more 8-bit words, labelled 'Data' in figure 2, with a corresponding 6-bit command, labelled 'Ctrl' in figure 2. Table 1 is a listing of the commands available for download to the FPGA. Three additional lines between the Rabbit and the FPGA are used to control the FPGA's overall operation. There is a data ready line used to strobe each command and data word into the FPGA. There is a start line, labelled 'Start' in figure 2, used to tell the FPGA to begin its active states. Finally, there is a reset line to place the state machine in its reset state. The Rabbit also sets several other parameters not directed to the FPGA. These parameters do not require the high-speed timing of the FPGA since they are seldom changed during a radar test. They are 3 bits to control 3 sets of attenuators, 1 bit to latch an attenuator indicator register, 4 bits to control the fine delay adjustment of a 10 MHz clock provided by the FPGA, and 1 bit for local/remote start source selection. Table 2 contains a summary of additional Rabbit commands either sent as control signals to the FPGA or not directed to the FPGA. Table 3 relates all the Rabbit commands to physical connections on the Rabbit I/O connectors and the corresponding pin names.

Currently, the simple user interface is replaced with a GUI written in HyperText Markup Language (HTML) and residing in the Rabbit. Now the Rabbit is treated as a web server, with a network connection to the PC. The user opens up a browser on the PC and connects to the GUI web page on the Rabbit to configure the timing parameters or load predefined ones.

Table 1. Rabbit Commands for FPGA

Command	Rabbit GUI label	FPGA code equivalent
1	State 1 duration	State 1 counter max
2	State 2 duration	State 2 counter max
3	Number of pulses per frequency	State 2 rep counter max
4	Number of frequencies	Frequency counter max, LSB
5	N/A	Frequency counter max, MSB
6	Transmit switch low	Transmit switch low going count
7	Transmit switch high	Transmit switch high going count
8	Transmit pulse low	Transmit pulse low going count
9	Transmit pulse high	Transmit pulse high going count
10	Transmit polarization delay	Change transmit pol. count
11	Initial polarization	Initial polarization
12	Pulses per polarization	Pulses per polarization
13	N/A (predefined in code)	Remainder for locating pol.
14	Rec. protection low	Rec. protection low going count
15	Rec. protection high	Rec. protection high going count
16	IF switch low	IF switch low going count
17	IF switch high	IF switch high going count
18	Detector sample low	Detector sample low going count
19	Detector sample high	Detector sample high going count
20	Video bias delay	Video bias low going count
21	Video bias duration	Video bias high going count
22	Frequency strobe delay	Frequency strobe low going count
23	Frequency strobe duration	Frequency strobe high going count
24	TWT blank low	TWT blank low going count
25	TWT blank high	TWT blank high going count
26	Frequency step delay	Frequency step low going count
27	Frequency step duration	Frequency step high going count
28	Pre trigger low	Pre trigger low going count
29	Pre trigger high	Pre trigger high going count
30	Accumulator clear delay	Accumulator clear low going count
31	Accumulator clear duration	Accumulator clear high going count
32	Phase delay	Change phase count
33	Initial phase	Initial phase
34	Phase increment	Phase increment
35	N/A	Number of freq steps, LSB
36	N/A	Number of freq steps, MSB
37	Start frequency	Start frequency, LSB
38	N/A	Start frequency, MSB
39	Frequency step size	Frequency step size, LSB
40	N/A	Frequency step size, MSB
41	ADC trigger control	ADC computer trigger, reset - bits1,0

Table 2. Remaining Rabbit Commands

Command	Comments
Select attenuation (dB)	Set attenuator bits
Read attenuator settings	Latch attenuator indicator bits
Set start control	Local FPGA control or remote (RS422) FPGA control
Output clock delay	10 MHz FPGA output clock delay (0-100 ns)
Download data to FPGA	Send all commands and current data to FPGA
Reset FPGA	Put FPGA in initial state
Run FPGA once	Send one start pulse to FPGA for one freq. sweep
Run FPGA forever	Start pulse always active to repeat freq. sweeps
Quit	Exit GUI

Table 3. Rabbit I/O for State Machine

Use	Rabbit Conn-Pin	Pin Name
6-Bit Commands for FPGA	J1-27 to J1-32	PD[7:2]
8-bit Data for FPGA	J1-3 to J1-10	PA[7:0]
DATA_READY	J1-23	PG0
START	J1-24	PG1
FPGA_RESET	J1-25	PG2
START_CTRL	J1-26	PG3
3-Bit ATTN CTRL	J2-17 to J2-19	PE3,1,0
6-Bit ATTN IND	J2-3 to J2-8	PB[7:2]
STROBE ATTN IND	J2-2	PB0
4-Bit Delay Clock	J2-13 to J2-16	PE[7:4]

3.4 Logic and Fine Timing Adjustment

Additional logic is provided on the main board to interface to the outside world and provide test points for trouble shooting, shown in table 4. Several timing signals require finer adjustment than the 25 ns allows from within the FPGA. These signals are routed into the fine timing adjustment section on the main board. This section consists of 3-bit delay chips with a resolution of 3 ns and programmable with dip switches. A 4-bit delay chip, programmable from the Rabbit GUI, is provided to adjust the 10 MHz clock from the FPGA in 10 ns increments.

Table 4. State Machine Test Point Connector. (a) Signal order (b) Pin order

signal order

Test Point Signal	Signal Label	Conn-Pin
Transmit switch	XSW1 (before delay chip)	P4-3
Transmit switch	XSW1 (after delay chip)	P4-4
Transmit pulse	XPUL (before delay chip)	P4-5
Transmit pulse	XPUL (after delay chip)	P4-6
Rec. protection	RPRO (before delay chip)	P4-9
Rec. protection	RPRO (after delay chip)	P4-8
IF switch	IFSW (before delay chip)	P4-11
IF switch	IFSW (after delay chip)	P4-22
TWT blanking	TWTB (before delay chip)	P4-19
TWT blanking	TWTB (after delay chip)	P4-20
Transmit polarization	XPOL	P4-7
Detector sample	DETS	P4-13
Video bias	VIDEOBIAS (OFFS)	P4-15
Frequency strobe	FREQSTROBE	P4-17
Frequency, lsb	FREQ0	P4-10
Phase, lsb	PHASE0	P4-12
Accumulator clear	ACC	P4-14
Pre trigger	PRET	P4-16
Data load (FPGA)	DATA	P4-21
Ground	GND	P4-1,2,25,26

pin order

Signal Label	Conn-Pin	Signal Label	Conn-Pin
GND	P4-1	GND	P4-2
XSW1 (before delay chip)	P4-3	XSW1 (after delay chip)	P4-4
XPUL (before delay chip)	P4-5	XPUL (after delay chip)	P4-6
XPOL	P4-7	RPRO (after delay chip)	P4-8
RPRO (before delay chip)	P4-9	FREQ0	P4-10
IFSW (before delay chip)	P4-11	PHASE0	P4-12
DETS	P4-13	ACC	P4-14
VIDEOBIAS (OFFS)	P4-15	PRET	P4-16
FREQSTROBE	P4-17	N/A	P4-18
TWTB (before delay chip)	P4-19	TWTB (after delay chip)	P4-20
DATA	P4-21	IFSW (after delay chip)	P4-22
NC	P4-23	NC	P4-24
GND	P4-25	GND	P4-26

4. Timing and Control

The timing of the state machine can best be described in terms of its four operating states, reset, idle, state1 and state2 as shown in figure 3, a state flow diagram. The first state, reset, is a unique state in that it will occur asynchronous to the input clock. A control line from the Rabbit activates the reset which will take the state machine out of any other state, reset parameters to initial conditions and then force the state machine's next state to idle. Idle is a clock synchronized state that also resets parameters to initial conditions. It is arrived at by either a reset of the state machine or by the completion of the final state1 state2 sequence. A start signal, in conjunction with the idle state will initiate state1, the first of the active states, that is, states where timing signals are changing.

The state machine has two active states, state1 and state2, where the timing signals are user configured to control the radar operation. The sequence during the active states is one state1 period followed by n state2 periods where n is the number of pulses transmitted per frequency. This sequence is repeated until all m step frequencies have been transmitted, at which point the state machine goes into idle state unless the start signal is still active (continuous run mode). Figure 4 shows the transition from idle to active to idle. The user can select the duration of state1 in multiples of 25 ns (rabbit command 1) to provide the required time for frequency changes, video bias adjustment, accumulator clear, etc. Currently, state1 duration is set to 1 us. The user also selects the duration of state2 in multiples of 25 ns (rabbit command 2) as well as the number of repetitions of state2, which is really the number of pulses per frequency (rabbit command 3). Currently, state2 duration is set to 1 us, corresponding to a PRF of 1 MHz, and the pulses per frequency is 16.

Control is provided within state1 for adjustment of the following signals: video bias, frequency strobe, frequency step, pretrigger, and accumulator clear. The timing adjustment available is indicated in table 1 as either a) a delay from state start and a pulse duration or b) a delay from the state start for the low going transition and a delay for the high going transition. Figure 5 clarifies the two methods of configuring the timing signal. It should be noted that the sole reason for providing two methods of defining timing signals is for clarity. If the waveform cannot be clearly expressed as a delay and a pulse duration in the GUI, then we selected the transition method. The method selected has no effect on timing resolution. In either case, timing adjustments can be made to 25 ns in resolution within the FPGA.

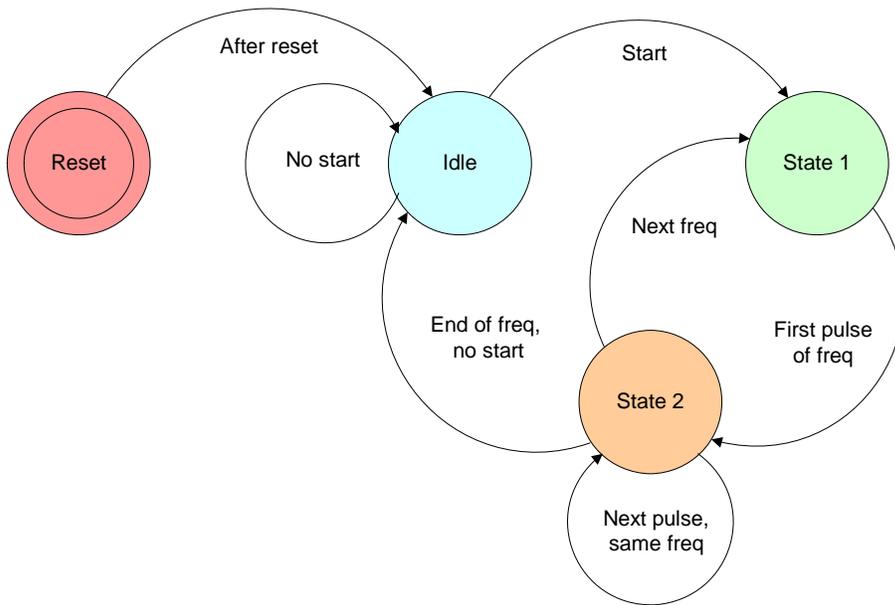


Figure 3. State flow diagram.

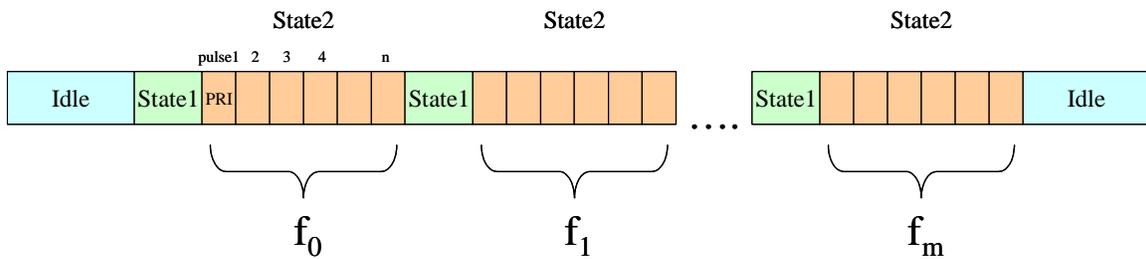


Figure 4. States of Operation for State Machine with m step frequencies and n pulses per frequency.

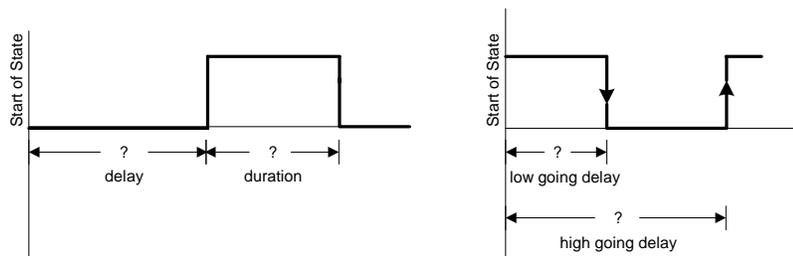


Figure 5. Two methods of timing signal configuration (a) delay and duration (b) low going delay and high-going delay.

Control is provided within state2 for adjustment of following signals: IF blanking switch, pretrigger, receiver protection, interpulse blanking 1 (transmit switch), interpulse blanking 2 (TWT blank), transmit pulse, detector sample and phase. Polarity change will also occur during state2, but usually only selected for every fourth or eighth transmit pulse. Table 5 lists the output signals that the user has control over and in which state or states that signal will have a transition. Predefined values are also shown for each signal, in the states where there is no transition. Transmit polarization is the only signal shown (also true for the phase word and frequency word) that the user can select the initial value for as well as the timing using the GUI interface.

In the case of the IF blanking switch, receiver protection, transmit switch, TWT blank, and transmit pulse, timing adjustments finer than 25 ns are available on the main board by means of dip switches controlling 3-bit delay chips. The delay chips, PDU13F by Data Delay Devices, Inc., have 3 address bits allowing 8 possible delays. The incremental delay will depend on the pin compatible version of the chip selected, varying from 0.5 ns steps (-.5 version) to 50 ns steps (-50 version). We selected 3 ns steps (-3 version) for our application. This version fits within the coarser FPGA adjustment of 25 ns allowing adjustment of 0 to 21 ns plus a chip propagation delay of about 6 ns. The IF blanking switch signal and the transmit switch signal each have one delay chip on the main board. Hence, we can adjust the delay of these signals in 3 ns steps. Receiver protection, TWT blank, and transmit pulse each have two delay chips on the main board. These signals can be fine tuned in both delay and pulse width. Table 6 provides a summary of the coarse and fine tuning possibilities for each of the timing signals.

Table 5. Predefined timing signal values and transition states

Signal	Label	Idle/Reset	State 1	State 2
Transmit switch	XSW1	1	1	pulse
Transmit pulse	XPUL	1	1	pulse
Transmit polarization	XPOL	initial	initial	1/0
Rec. protection	RPRO	1	1	pulse
IF switch	IFSW	1	1	pulse
Detector sample	DETS	0	0	pulse
Video bias	OFFS	0	pulse	0
Frequency strobe	FREQSTROBE	0	pulse	0
TWT blank	TWTB	1	1	pulse
Frequency step	none	0	pulse	0
Pre trigger	PRET	1	pulse	pulse
Accumulator clear	ACC	1	pulse	1

Table 6. Coarse and fine tuning resolution in nanoseconds for timing signals

Signal	Coarse Adj.	Fine Adj.	Fine Adj. Type
Transmit switch	25	3	D
Transmit pulse	25	3	D/PW
Transmit polarization delay	25		
Rec. protection	25	3	D/PW
IF switch	25	3	D
Detector sample	25		
Video bias	25		
Frequency strobe	25		
TWT blank	25	3	D/PW
Frequency step	25		
Pre trigger	25		
Accumulator clear	25		
Phase delay	25		
A/D clock		10	D

D=Delay, PW=Pulse Width

5. Operation

The operation of the FPGA portion of the state machine was simulated with a VHDL testbench program and the actual state machine VHDL code using ModelSim. The startup portion of the timing diagram is shown in figure 6 consisting of approximately one step-frequency cycle. The start command causes the state machine to enter state 1 (see “current state” signal) where timing signals for pretrigger, video bias, frequency strobe and accumulator clear are activated. Upon completion of state 1, whose duration was set to about 1 us in the simulation, state 2 begins, causing the remaining signals to become active after their respective, programmed delays. There are 16 repetitions of state2, each of which is about 1 us in duration. During each repetition, a transmit pulse is generated along with supporting signals receiver protection, transmit switch, TWT blanking, IF switch and detection sample. Phase is incremented (by one in our example) every state 2 repetition. Polarization, on the other hand, switches every fourth occurrence of the transmit pulse.

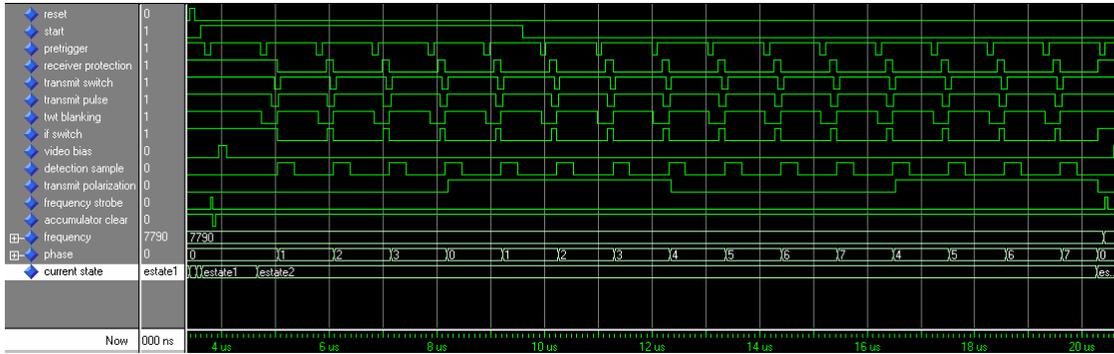


Figure 6. Timing diagram from simulation.

6. Board Layout

The main state machine board is constructed of 62 mil, FR4, double sided, 1/2 oz copper board material. It was designed and laid out in-house using Protel DXP 2004 and routed on a routing machine. The Rabbit CPU board is mounted on top of the state machine board in a “daughter-card” configuration. The signals are transferred between the two boards through two 34-pin connectors. The APS-V240 FPGA board is also mounted atop the state machine board with three 50 pin ribbon cables bridging the gap between three connectors on each board. The schematic of the state machine board is shown in figure B1. Figure 7 gives an approximate block diagram of the layout while figure 8 shows a photo of the completed and populated board. The actual printed circuit board layout is shown in figure B2.

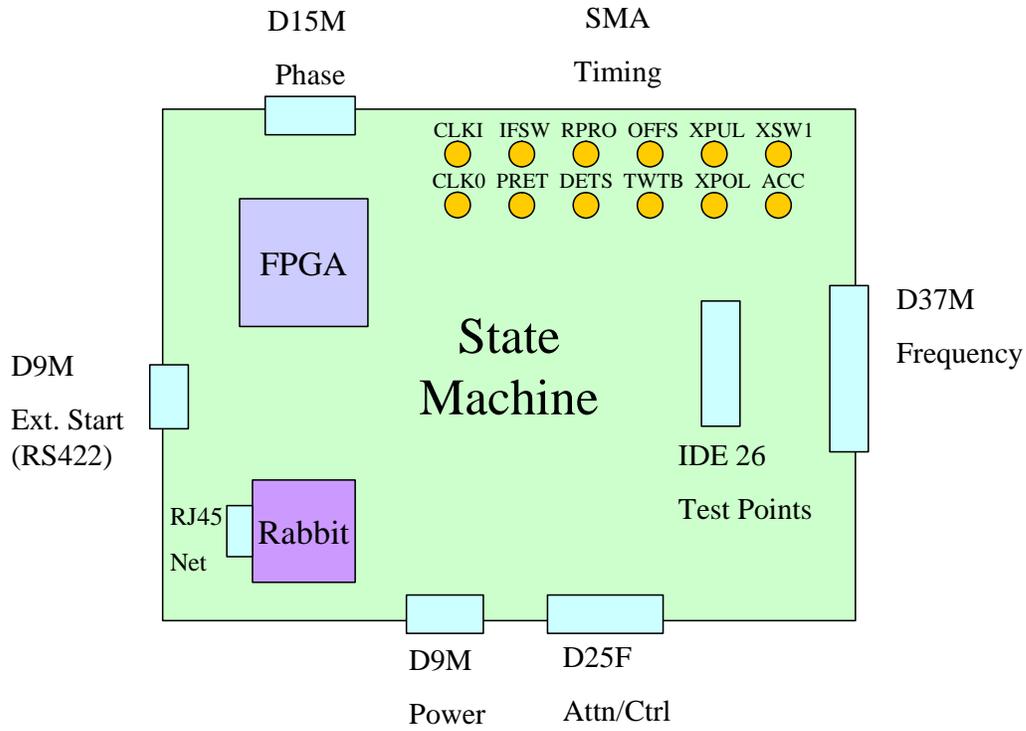


Figure 7. State Machine Board Block Diagram.

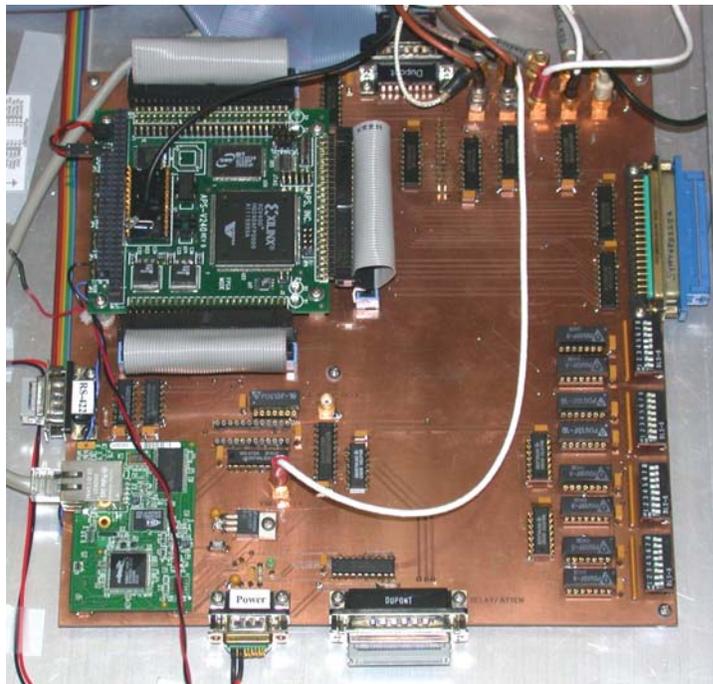


Figure 8. Photo of Completed State Machine Board.

7. Summary

A new state machine board has been designed, built and successfully tested for the Ka-Band instrumentation radar. The board provides the necessary timing signals to the RF section to control transmit pulse width, receiver protection switches, and the polarization switch. It also provides the IF section with an IF switch control, a video bias control and up to 8 bits of phase control. It provides the frequency synthesizer board with 15-bit frequency data and a signal to strobe it into registers. Finally, it provides the data acquisition system with a signal to begin sampling incoming data. Resolution of the timing signals has improved from 100 ns for the previous state machine board to 25 ns for the new board. The more critical signals can be fine tuned to a few nanoseconds with on-board delay chips. Perhaps, most significant of all, is that unlike the previous design, this state machine can be reconfigured during operation, allowing timing adjustments, adjustment to the number of frequencies and step size, changes to starting phase and phase increment. It will eliminate significant down-time for reconfiguration while providing a flexible interface for user control.

Appendix A - Ka Band Radar System Parameters

Operating frequency (fo)	35 GHz
Bandwidth	3 GHz
Integration	8 pulses
Number of channels	12
A/D resolution	12 bits
PRF	1 MHz
Rotation Time	10 minutes
Range Gate Length	15 meters

Appendix B - Interconnect Schematic/PCB Layout

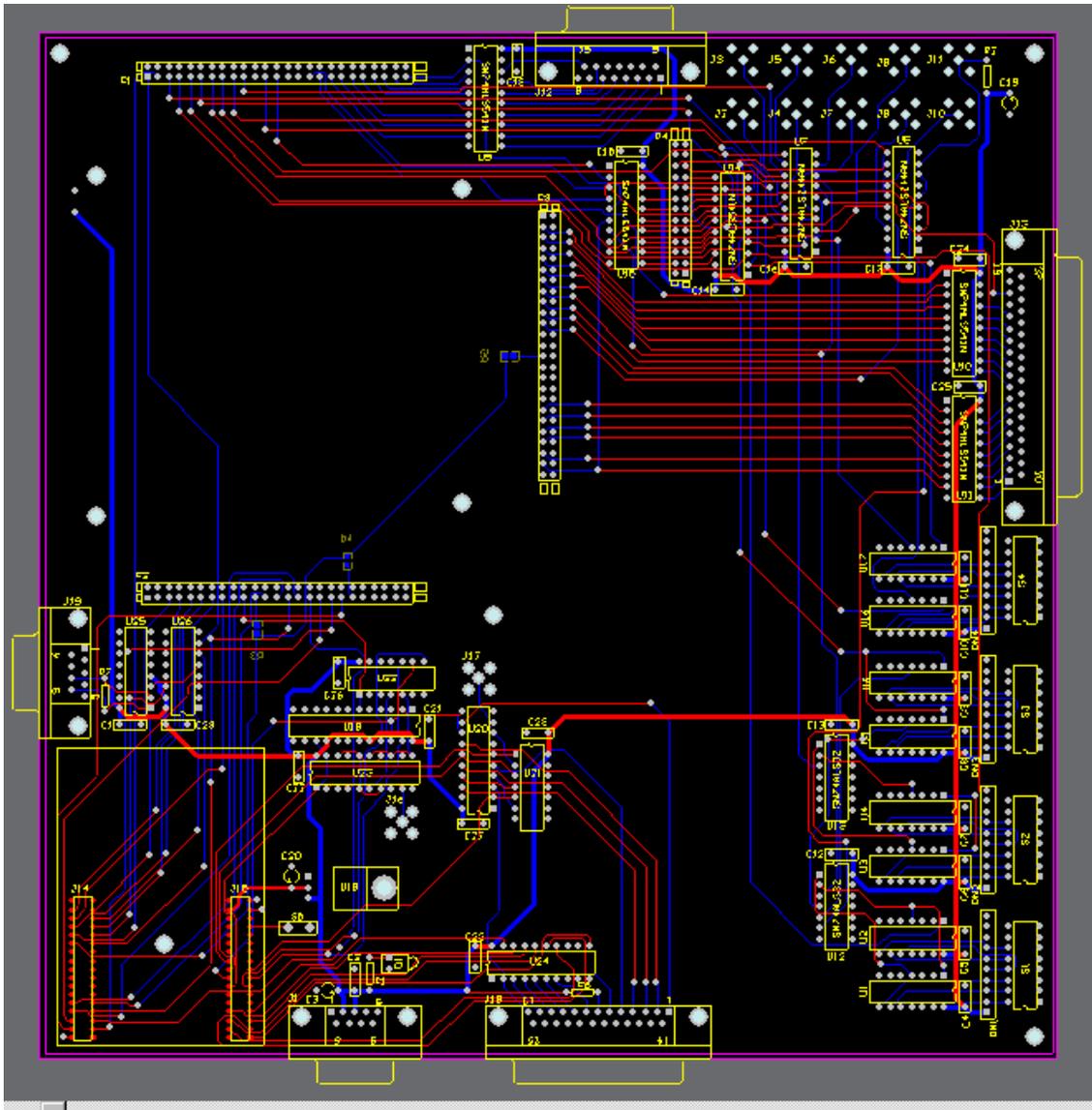


Figure B2. PCB Layout of State Machine.

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