Flip Chip Bonding of 68x68 MWIR LED Arrays

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14. **ABSTRACT**  
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15. **SUBJECT TERMS**  
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Index Terms—Flip-chip bonding, LED array, CMOS drivers, contact resistance

I. INTRODUCTION

Passive IR imaging and IR detector arrays for seekers play a very important role in missile defense operations and systems as well as for other DOD applications. The seeker testing requires large 2D arrays, high frame rates and large dynamic range IR sources. Several IR sources have been integrated into the hardware in the loop (HWIL) facility in the past, including a scanning laser array, resistive array and digital micro mirror devices (DMD) [1]. We have shown in an earlier publication that mid-wave infrared (MWIR) light emitting diodes (LED) can be used for IR scene generation [2]. MWIR light sources are of growing importance because of applications in infrared scene generation, infrared counter measures (IRCM), spectroscopic chemical and biological threat monitoring, medical diagnostics and gas sensors.

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MWIR LED’s are desirable for many such applications because of considerable advantages in terms of low cost, small volume, long term reliability, broad spectral content, and fast switching speed. For MWIR region (3-5 μm emission wavelength) GaSb based substrate material is preferred. The transmission of IR light through GaSb material varies between 5-30% and depends on the type of substrate dopants (n- or p-type). Hence for bottom emitting LED devices, it is desirable to remove the bulk of the GaSb substrate material to acquire sufficient light from the device active region.

For IR scene generation applications, the LED devices are required to simulate very high temperature targets on the order of 3000K apparent black body temperature. Hence, the goal is to fabricate LED devices maximizing light output for a particular epitaxial design structure. Heat dissipation is also another important factor in designing a MWIR LED array. One possible method to achieve low contact resistance and good thermal conductivity is to use flip-chip technology [3-5]. Flip chip hybridization is a packaging technique whereby a chip is attached to a substrate facedown eliminating peripheral wire bonding. A grid of solder bumps on the surface of the active area of the die is joined directly to a corresponding set of solder bumps on the substrate. This will shorten the thermal path between the active light emitting region of LEDs and heat sink. Flip chip bonding of IR detectors with read-out integrated circuits has been extensively reported [6, 7]. High (force) pressure thermal compression [8] as well as low (force) pressures bonding with solder reflow with epoxy underfill [9] are used for flip chip bonding. However, very few published reports are available on flip chip bonding of LEDs to CMOS read-in integrated driver circuits [10]. Unlike single indium bump on silicon readout circuit in [3], we used two bumps, one on readout array side and other on LED array side. In this paper we report our experimental findings of a detailed optimization procedure for flip chip bonding of 68x68 MWIR LED arrays onto Si-CMOS driver arrays. Optical and electrical properties of the fabricated LED array will
II. EXPERIMENTAL

For this experiment we used super lattice light emitting diode (SLED) structure, consists of 16 cascaded MWIR super lattice emission regions (8.9/16 monolayer’s (ml) InAs/GaSb) separated by (n InAs/GaSb super lattice grade)/ (p+ GaSb) tunnel junctions. Graded super lattices were introduced between the GaSb clads and the first and last MWIR super lattice emission regions in order to smooth out interfacial spikes in the real space band structure. The structure was capped with a thin layer of p++ type GaSb, which has favorable band offsets for Ohmic p-contacts, blocks electrons from reaching the semiconductor-air surface, and is nominally transparent for reflection of emitted light off the top contact.

Device fabrication started with inductively coupled plasma (ICP) dry etching to define the mesa area. The square mesa size was 75 µm. The etch depth for mesa isolation was 3.0 µm. A silicon nitride layer of 3000 Ang. was then deposited by plasma enhanced chemical vapor deposition (PECVD) technique. Contact windows were opened in the Si3N4. A contact Ti/Au metallization was done by electron beam evaporation for both the top and bottom contacts. A chromium/ indium vacuum-thermal evaporation was the last photolithography step. A 300 angstroms of chromium immediately followed by 5 microns of indium was deposited on the LED arrays. The resulting deposition gave indium solder bumps 5 microns in height by 15 microns square. Two indium bumps per pixel, one on the cathode and the other on the anode were deposited. The total number of indium solder bumps for each 68 x 68 LED array was 9248. The same procedure was used to place indium bumps on the CMOS drivers. An LED device was then flip chip bonded to a corresponding CMOS driver, epoxy under filled, and the GaSb bulk substrate then removed. The 68x68 LED array has 8.4 mm² square area. Fig. 1 shows a schematic cross-sectional view of the flip chip mount LED array.

After flip chip bonding of LED array onto CMOS array, we removed the bottom GaSb substrate material by lapping and the light emission is observed through the substrate side [11]. We measured device IV characteristics before and after lapping. The IV characteristics do not change with lapping the substrate as both the anode and cathode contacts are on the top surface.

The size of the 68x68 CMOS driver array (Fig. 2) is 9.5 mm². The driver array was fabricated in the 130nm IBM 8HP SiGe process. Although the 8HP process is suited for high speed designs, this process was ultimately chosen for the high current densities afforded by the copper interconnect layers. The unit cells were designed to source up to 100mA to the LED, be individually addressable, and have analog drive and memory that can operate at a 1 kHz array refresh rate. Each unit cell contains a CMOS logic switch, a capacitor and a SiGe HBT driver. The switch is controlled by row and column select lines, which when activated charges the capacitor. The voltage stored on the capacitor controls the output current from the driver to the LED. Each unit cell (Fig. 2 b) contains a CMOS logic switch, a capacitor and a SiGe HBT driver. The cells have a 120 micron pitch and contain two 15 micron square pad openings for the anode and cathode contacts to the LED. The CMOS switch in each cell enables individual addressability of the LED driver array. The switch is controlled by row and column select lines, which when activated charges the storage capacitor to a variable input voltage.

Fig.2. (a) CMOS driver array and (b) single driver pixel

Pictures of the (68x68) LED array and single pixel LED pixel are shown in Fig. 3. The pitch size of the LED array is kept 120 micron to minimize the cross talk between individual LED pixels. As seen from the single pixel, the indium bump is deposited on cathode and anode pads. Since we are observing light from the bottom side of the substrate, the complete mesa area is covered by a Ti/Au metal layer. A thick
positive photo resist AZ 4620 of 8 μm thickness is used for Indium metal deposition and lift off process. For flip chip bonding we used Karl Suss FC150 flip chip bonding machines. After flip chip bonding, the GaSb substrate from the bottom side of the device is thinned by lapping and polishing. The final thickness of GaSb substrate is measured by optical microscopy as well as by a Fourier transform infrared (FTIR) spectrometer and is found to be 50 μm.

Fig. 3. (a) Photograph of 68x68 LED array and (b) single pixel LED

In Figure 4, we have shown the picture of LED array flip chip onto CMOS driver. Wire bonding is done between the bonding pads in CMOS array and the pads on the ceramic package. There are test LED devices at the four corners, which can be tested directly without going through the Si-CMOS driver circuits. These devices are used to measure the single LED performance as well as to monitor the flip chip bonding process. Besides four corners LED test pads, there are 296 bonding pads in CMOS driver to bias each LED pixel independently. The array is mounted on an electronic driver board which supplies various biasing voltages and the light output is measured by using SBIR 320x256 InSb focal plane array camera. We use 2 inch ZnSe lens to focus the LED picture onto IR camera.

Fig. 4. Photograph of LED array flip chip mounted on to the CMOS drive array.

II. RESULTS AND DISCUSSIONS

The spectra of light emission from LEDs are measured by Fourier transform infrared (FTIR) spectroscopic technique. Fig. 5 shows the room temperature spectra of light emission from the LED device with 16 cascade layers with two injection current levels. The luminescence spectra of the device peak at 3.8 μm. There is very little peak wavelength shift for injection currents of 5 and 15 mA. This may be due to the small difference in injection current levels.

Fig. 5. MWIR LED spectra at two injection currents

We performed flip-chip experiments varying bonding pressure between 3 Kg and 11.5 Kg. We used Karl Suss FC 150 flip chip bonding machine for flip chip experiments. The results of the bonding experiments in the FC 150 machine are shown in Fig. 6. First for optimization experiments, we used test chip array with only metal pads and two indium bumps for each pixel. Similarly we also use a test chip for driver side with metal pad and indium bumps. We measured the continuity of bonding by measuring the resistance at two test pads in driver side of the test chips. After the flip chip bonding we pulled apart the test chips and then took SEM picture of the pad area. We performed experiments with bonding at room temperature and 100 °C. We also varied the bonding time between 60 to 300 sec. This is the time for which the bonding pressure was applied. For 100 °C bonding sample forced air cooling was used to cool up to 80 °C and then normal cooling cycle was used.

As it is seen in Figure 6 (a)-(b) the bonding was done with 8.5 Kg pressure either at room temperature or 100 °C bonding temperature and 60 sec bonding time. The SEM pictures show good contact and very low deformation of indium bumps. In case of the
samples (c) and (d) the indium pads are deformed heavily and may result in shorts in large array. By comparing Fig. 6 (a) and (b), the SEM picture shows similar deformation of the bonding pads and the spreading is acceptable. Since we do not want the indium bump to be deformed due to high temperature stress, we limit the bonding temperature much lower than Indium melting temperature (156.7 °C). However, we have also done contact resistance measurement (not shown here) and found that sample (b) has lower resistance than sample (a). It may be due to fact that at higher temperature Indium oxide breaks down easily and hence causes low contact resistance. Hence we used 8.5 Kg pressure, 100 °C bonding temperature and 60 sec bonding time for all the arrays the results of which is presented in this paper. The applied pressure is equivalent to approximately 1 gm per bump which is higher than previously reported results [12]. This may be due to the fact that we have two bumps per pixel where the authors in the paper [12] have used single bump per pixel.

We measured the current voltage (I-V) curves for devices before flip chip bonding and after flip chip bonding. The voltage drop is about 4 V at 5 mA injection current, which is typical for 16 stage SLED structure. As seen in Figure 7, the I-V curves look similar which indicates that the resistance increase due to flip chip bonding is negligible. We observed very little increase in voltage drop in the device at low injection current levels. However, the voltage drop at higher injection current level is little higher for flip chip devices. Though we have shown here results from two devices, we observed uniform IV curves from LED devices at four corners of the array. In an earlier paper [2], we have shown that the peak wavelength of emission shift to higher wavelength for higher injection current densities.

Figure 6. SEM picture of indium bump with different flip chip conditions (a) 8.5 Kg/RT/60sec, (b) 8.5 Kg/100 C/60 sec, (c) 8.5 Kg/100 C/300 sec., and (d) 11.5 Kg/ 100 C/60 sec.

Figure 7. I-V curves for device before and after flip chip bonding

We used a Santa Barbara Infrared (SBIR) 320x256 InSb focal plane array camera for observing the light emission from the LED array. The camera has a liquid nitrogen pour filled dewar and operates at 77 K. A ZnSe two inch focal length lens is used to magnify the LED array while taking pictures using the IR camera. The array is mounted onto a 68 pin LCC package and kept in the dewar for biasing the
devices. As seen in figure 8, LEDs at three corners of the 68x68 array are emitting light. The LED at the fourth corner was not working before flip-chip bonding and hence we don’t expect to see the light from this LED. Form the light emission pictures, we concluded that the flip chip process results in good contact between CMOS driver and LED array.

Figure 8. Photograph of MWIR LED emission at three corners of the array.

We took a photograph of light emission from one of the corner LEDs of the array. We used a one inch focal length ZnSe lens for this figure which is different from 2 inch focal length lens used for Figure 8. The injection current was 10 mA and the voltage drop across the device was 5.5 V. The background at the corner of the LED array is also seen in picture. We also took the surface plot of the light emission across the LED and have shown in Figure 9 (b). Though we expect the picture to be square, because of focus error the pixel looks circular. The light emission is quite uniform across the LED mesa area and also goes down to background level outside the mesa area.

Figure 9. (a) MWIR camera picture of single LED, (b) Surface plot of the light emission from single LED

Figure 10. Picture of light emission from full array

In Figure 10, we have shown the light emission from complete 68x68 LED array. We have not tried to light the entire array because not all the wire-bonds for power pads are connected. Though we need approximately 290 pads for biasing the complete array, we have only 68 pins available from the LCC package. In few cases we have double the wire bonds from LED array to each pad on LCC package. The picture shows very good contact across the array and approximately 90% of the LEDs in the array are emitting lights. It may be noted that few center rows/columns are not accessible due to number of available bonding pads and they are seen dark for that reason.

III. SUMMARY

The MWIR LED arrays were flip chip bonded onto a Si-CMOS driver array. Both the LED and CMOS driver arrays have indium bumps which were deposited by a thermal evaporation technique. We used a thermo-compression technique to flip-chip bond the LED and CMOS driver arrays. On the basis of contact resistance and change in bump shape after flip-chip bonding the accurate bond pressure, time
and temperature are found to be 8.5 Kg, 60 sec. and 100 C respectively. The arrays are lapped and polished after flip chip bonding and before mounting on to the LCC package. The device electrical IV characteristics as well as optical emission characteristics were measured. Since we have two bumps per pixel (anode and cathode contacts) approximately 1 gm per bump is required for flip chip bonding. Though we have presented the results from room temperature measurements, we intend to carry out cryogenic testing of the LED arrays and expect the flip chip bonding process will not have any degrading effect on contact resistance. We have not tried soldering reflow technique for flip chip bonding and hope similar experiments will be more rewarding.

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