Power for Microsystems

by Brian Morgan, Sarah Bedair, Christopher Meyer, Christopher Dougherty, Lin Xue, David Arnold, Rizwan Bashirullah, Jeffrey Pulskamp, and Ronald G. Polcawich

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Power for Microsystems

Brian Morgan, Sarah Bedair, Christopher Meyer, Christopher Dougherty, Lin Xue, David Arnold, Rizwan Bashirullah, Jeffrey Pulskamp, and Ronald G. Polcawich
Sensors and Electron Devices Directorate, ARL
This report details progress on developing cubic millimeter power converters in an attempt to bridge the gap between sources and loads in emerging military microsystems. A multi-pronged approach has been pursued that includes fundamental modeling of high frequency converter topologies that are necessary to achieve the desired size scale while also addressing the myriad voltage and power requirements envisioned. Prototype converters have been designed and tested, demonstrating state-of-the-art conversion ratios for such devices. The high converter operation frequency used enabled the development of high performance micro-electromechanical system (MEMS) passive components that demonstrated similar performance to commercial-off-the-shelf (COTS) inductors while offering up to a 10 times reduction in area and a 100 times reduction in volume. Parallel research paths have emerged, including the development of a novel nanoparticle self-assembly technique capable of creating high frequency capacitors and inductors without resorting to complicated fabrication sequences or high temperature processing. We have also leveraged close collaborations within the U.S. Army Research Laboratory (ARL) to develop piezo-MEMS resonant transformers, which hold tremendous potential for micron-scale point-of-load conversion while maintaining or exceeding the high power densities achieved at larger scales. In total, this research has demonstrated key enabling technologies for efficient power distribution within compact military systems at the cubic millimeter scale while maintaining competitive efficiencies and handling relevant voltages.
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1. Introduction/Objective

The U.S. Army Research Laboratory’s (ARL) Micro Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA) program is focused on developing autonomous mobile microsystems to enhance tactical awareness in urban and complex terrains. These systems are projected to be palm sized and smaller to provide a combination of stealth and accessibility to restricted areas, as well as to improve portability for the Soldier and enable cooperative group behavior for superior mission capability. As with larger scale robots, these systems will ultimately be limited by the available power and energy onboard. Due to their high power density, lithium polymer (LiPo) batteries often serve as the backbone of these systems since they can provide the 10–100+ W/kg (Autumn, 2006; Steltz, 2006) that may be required for small robotic platforms. While the energy density of a LiPo drops off at high drain currents (Stux, 2007), their capacity is generally sufficient for missions in the tens of minutes range (platform dependent) if it can be delivered efficiently.

Creating mobile systems then requires power dense and efficient motors or actuators to transform electrical power into mechanical work for locomotion. However, at small scales, the power density and efficiency of traditional actuators become limited and/or impractical, whereas devices like piezoelectric actuators become more favorable (Karpelson, 2008). Since piezoelectrics require high voltages, power distribution to the “motor” as well as the wide variety of sub-systems on this tiny platform begins to resemble a small “pico-grid,” where each load may require vastly different flavors of power (1–100+ V, µW to W), as illustrated in figure 1 (Morgan, 2010). The vast range of potential power consumers obviates the need for efficient miniature power conversion and management solutions; implementation of commercially available converters for a mm³/mg-scale autonomous system would cripple the mobility of such scaled platforms. The “Power for Microsystems” Director’s Strategic Initiative program was therefore initiated to focus on this critical gap between miniature power sources and loads in emerging microsystems. This report outlines the approach taken in our research and highlights the results of our work in high frequency circuits and micro-electromechanical system (MEMS) passive components.
2. Approach

Producing miniature power converters requires advancements in circuits, passive components, materials, and packaging/integration. Thus, our technical approach is multi-pronged:

- First, we are developing new complementary metal-oxide semiconductor (CMOS) converter architectures for the unique requirements of miniature mobile systems. Primary design considerations for boost converters include efficient conversion using circuits that are small in size and have the ability to create and process high voltages in conjunction with large conversion ratios. High operating frequencies in the range of 10–200 MHz are therefore required to enable on-chip or over-die integration of passive components. Since, under fixed ripple constraints, component size decreases as a function of 1/frequency squared, significant reduction in overall volume and size should be possible. To address the increased switching losses at higher frequencies, research is required to identify circuit techniques and architectures that enable component integration without requiring a large penalty in terms of efficiency.
• Second, we are leveraging our expertise in MEMS to microfabricate ultra-miniature passive components for the high frequency circuits. In a power converter, the role of a switched inductor is to store energy magnetically in its core and then deliver this energy electrically to a load. The quality factor of an inductor, a measure of how well it stores versus dissipates energy, given by $Q = \omega L/R$, indicates that optimum efficiency can be achieved by increasing the operating frequency, $\omega$, and inductance, $L$, while decreasing resistance, $R$. The resistive term includes the electrical resistance of the conductor, eddy current, and magnetic core losses. Typically, high permeability cores have been implemented to drastically increase inductance. However, problems in producing microfabricated, cored inductors have included high processing temperature, core losses that increase rapidly with frequency, and permeabilities that degrade at higher frequencies (Gardner, 2009). Therefore, in high-frequency applications, air-core inductors may have an advantage in terms of cost, fabrication simplicity, weight, and power loss over traditional high permeability core inductors, and thus, have served as the focus of our work. While air-core works well for inductors, high voltage MEMS capacitors remained a challenge. Thus, we initiated an investigation into nanoparticle material deposition at the micron scale to address this gap. This new self-assembly technique was used to fabricate both capacitors and inductors capable of maintaining high performance up to the >200 MHz regime as desired for the power converters in development.

• Finally, in collaboration with other groups at ARL, we are investigating a completely new converter paradigm based on piezoelectric MEMS (piezo-MEMS) resonators to enable transformers with 10–100 times size reduction compared to the state of the art (SoA). While these devices will require new circuit architectures, their inherent power densities are extremely attractive and they offer the potential for superior point-of-load voltage converter integration with various MEMS switches, filters, and sensors already in development. Section 3 provides further detail on the technical progress in each of the areas identified previously.

3. Results

3.1 Mm-scale Converters

To miniaturize power converters to the required size scale (preferably, milligrams), we are increasing the frequency of traditional switch-mode CMOS converters (100+ MHz versus 1–10 MHz) while incorporating design features to improve high voltage handling on the CMOS chip. Extensive modeling and prior art has shown that achieving the tens of volts required to drive piezoelectric actuators is best achieved by driving a switched-capacitor ladder stage with a switched-inductor boost stage (Steltz, 2006; Li, 2010).
While one could certainly move to exotic foundry processes (like silicon-on-insulator [SOI] or III-V), we chose to start by investigating the bounds of possibility in readily available standard 130-nm, 1.2-V CMOSs. The use of standard CMOS technologies is also well suited for integrating radio frequency (RF) and digital subsystems for communication and signal processing functions in a miniature footprint. Processing of the large voltages within an inherently voltage limited technology was enabled by the development of devices such as custom Schottky barrier diodes (SBDs) and stacked negative metal oxide semiconductor (NMOS) synchronous switches. CMOS-compatible SBDs that support blocking voltages of 10 V in a 1.2-V process are fabricated by selectively blocking the n+/p+ implants in desired diffusion areas or directly contacting the N-/P- well with metallization (Li, 2010). A further increase in blocking voltage is established by isolating each switched-capacitor (SC) stage from the substrate, creating independent voltage “islands”—a technique compatible with fully depleted SOI processes. Moreover, the step-up ratio of traditional switch-mode boost converters is generally limited by realizable duty cycle and parasitic losses of the inductor and power train stages. Here, we describe a 25–120 MHz hybrid switched-inductor (SI) SC DC-DC boost converter that provides a 36-V output from a 1.2-V input (a conversion ratio of ~30) fabricated in 0.13-μm bulk CMOSs.

Figure 2 shows the architecture of the hybrid SI/SC DC-DC boost converter. The SI stage with a COTS L=220 nH and Q~25 uses a stacked NMOS low-side switch to create a square-wave output at the switching node, Vx, driving the input of the diode-multiplier SC converter. The switch is made with a 3.3-V, 70-Å thick-oxide NMOS stacked on a low-V_T thick-oxide NMOS device for large breakdown voltage. Measurement results show that on-conductance is 1 Mho/cm with a breakdown of >10 V. The N=4 stage multiplier is composed of on-chip metal-insulator-metal (MIM) capacitors and p-type Schottky diodes fabricated in isolated p-wells (enclosed in deep n-well) by selectively blocking p+ implants in desired diffusion areas (Li, 2010). Assuming a duty cycle D, the voltage conversion ratio can be approximated as V_{out}/V_{in}~N/(1-D). A large conversion ratio is achieved while limiting the voltage stress on any individual switch, diode, or capacitor, making this hybrid topology suitable for integration in a low-voltage CMOS process. Since hysteretic control is not traditional for the boost converter, a new hysteretic pulse width modulation (PWM) controller was developed (also shown in figure 2), designed for quick transient response, simplicity, and unconditional stability. A high switching frequency of 25–120 MHz was explicitly chosen to minimize the size of passive components, thus limiting the inductor of the SI stage to 220 nH and the total capacitance of the SC stages to <2 nF. An output-equivalent-impedance-based optimization algorithm was used to minimize the total area of the SC converter (Seeman, 2008), wherein each successive SC stage uses less overall capacitance that the previous stage.
The output voltage of the hybrid SI/SC boost converter was evaluated using a variable duty-cycle external switching clock of 25, 50, and 100 MHz for an output load of 520 kΩ (about half of a typical piezo-actuator load) and $V_{IN}$ of 1.2 and 3 V. Peak output voltages of ~13 and ~14 V were measured for $V_{IN}$=1.2 and 3 V, respectively, when $D>60\%$ and $f_{sw}=25$ MHz. Two possible breakdown mechanisms are likely to limit the peak output voltages. The first is the reverse breakdown of the SBD itself and the second is the parasitic pn junction between the p-substrate and deep n-well. In order to increase the output voltage handling, individual “voltage islands” were created by a physical post-process removal of the substrate between each SC stage, thereby limiting the blocking voltages to that of the step-up ratio produced within each SC stage. The resulting output voltages versus duty cycle are shown in figure 3 (left), with output voltages of 36 and 43 V for a 1.2- and 3-V input, respectively. In all cases, peak output voltages are obtained at 25 MHz, indicating a fast switching limit for the SC converter.
Figure 3 (right) shows the measured efficiencies versus load current for the hybrid converter with isolated SC islands under closed loop configuration for a 3-V input. The converter delivers a maximum load current of 650 μA at 10 V and 1100 μA at 20 V for 1.2- and 3-V inputs, respectively. For a 1.2-V input, the peak efficiency is 33% for 10-V output (I_L=250 μA, f_{sw}=50 MHz) and 25% for 20-V output (I_L=240 μA, f_{sw}=25 MHz). For a 3-V input, the corresponding peak efficiency is 36% for 20-V output (I_L=820 μA, f_{sw}=50 MHz) and 29% for 30-V output (I_L=500 μA, f_{sw}=50 MHz). The peak efficiency for both 1.2- and 3-V inputs occur at f_{sw}=50 MHz due to the SI stage.

Figure 4 (left) shows a comparison of the conversion ratio versus input voltage for recently published integrated boost converters. This work achieves the highest conversion ratios of ~11 (without substrate isolation) and ~30 (with substrate isolation) reported to date in a 0.1-μm, 1.2-V CMOS process. The hysteretic PWM controller occupies 0.84 mm², with a core active area of 0.06 mm². Total area of the SC stages is ~3 mm², dominated primarily by the integrated MIM capacitors (capacitance density of ~1 fF/μm²). Figure 4 (right) also shows representative timing waveforms for the hybrid SI/SC boost converter when driving a 12-V, 110-Hz resonant piezo-actuator fan that has an equivalent leakage resistor of 1 MΩ and load capacitor of 90 nF. The output voltage tracks the applied input voltage reference (V_{REF}) to produce a switching signal of ~120 MHz with a duty cycle of ~55%. The converter induces a displacement in the piezo-actuator of ±3 mm and dissipates ~14 mW.
Figure 4. Comparison of achieved conversion ratio in the literature (left) and the scheme used to drive a piezoelectric fan with our high voltage boost converter (right) ([4]=Li (2010), [6]=Richelli (2007), [7]=Richelli (2004)).

3.2 MEMS Passives

The converters described previously primarily used a 220-nH COTS inductor, which in its current format dwarfs the rest of the components. However, integration of power inductors has remained elusive due to the complexity of processing materials for magnetic cores (Mathuna, 2005) and the prohibitive core losses at high frequencies (Gardner, 2009). Therefore, we have developed new MEMS techniques to microfabricate ultra-miniature air-core inductors with high inductance densities and quality factors (Meyer, 2010a).

We have developed a four-layer, through-mold, electroplated-copper process for air-core inductors on Pyrex substrates (Meyer, 2010a). For the build-up of each layer of the process, copper seed layers of 200 nm thick were first deposited as the conductive starting surfaces onto which thicker layers of copper would be electrodeposited. Photoresist patterned on top of seed layers formed the plating mold and electroplating steps were timed so that the copper filled up to the top of the mold. Each copper winding layer is electroplated up to 10 µm thick for lower resistance than would be possible if the inductors were integrated in the metal layers of a CMOS process (Mathuna, 2005). The built-up four-layer structure was then released in photoresist developer to selectively etch certain exposed regions while leaving unexposed regions as structural elements separating the upper and lower copper windings. A square spiral three-dimensional layout was chosen to maximize inductance density. Although magnetic cores have typically been used to increase inductance, we leverage the enhanced mutual coupling of vertically stacked spirals to obtain high inductance densities without the integration incompatibilities associated with magnetic core materials. Because all steps are performed at low temperatures (< 95 °C), our process could enable CMOS back-end integration of inductors on-
chip. Scanning electron microscope (SEM) images of the fabricated inductors are shown in figure 5.

![SEM image of inductor structure](image)

Figure 5. Freestanding 0.5 × 0.5 mm micromachined inductor structure.

Through the abovementioned microfabrication-enabled advances, our air-core inductors achieve quality factors of >20 and inductance densities of >100 nH/mm² (Meyer, 2010b). As shown in figure 6, our inductors deliver not only higher inductance densities than most other microinductors—they also achieve high quality factors at frequencies that are not met by either magnetic thin films (Gardner, 2009) or GHz RF air-core devices. The measured DC resistance of the fabricated inductors range from 0.55–2.9 Ω and the max current capacity was experimentally determined to be ~450 mA. The same process also enabled air-core transformers with offering not only high coupling but also the opportunity for turn ratios greater than unity for voltage or current gain. Three transformer designs were fabricated and tested, all with areas 2.25 mm² and primary inductances of 47 nH but with variable secondary inductances to yield voltage gains from 1:1 up to 1:3.5. Load-dependent transformer performance characteristics were predicted from the 50-Ω-load measurements using network analysis techniques. The 1:3.5 step-up transformer projected a maximum efficiency of 78% around 150 MHz, while the isolation transformer had a projected 91% efficiency with a voltage gain of 0.95.

![Comparison of microfabricated inductors](image)

Figure 6. Comparison of microfabricated inductors. Bubble size is proportional to inductance density.
To demonstrate that our MEMS inductors can perform in a high frequency DC-DC converter, we used a hybrid boost converter composed of a SI stage followed by a two-stage SC charge pump. A microfabricated 14-nH inductor (Q=7.9 at 100 MHz) was assembled in a custom-printed circuit board and tested within the PWM controlled hybrid boost converter circuit. The converter (fabricated in a 130-nm, 1.2-V CMOS process) operated at ~100 MHz using either the COTS inductor or a microfabricated air-core inductor. Looking at figure 7, the performance using a non-optimized MEMS inductor is quite similar to that using the COTS device, while providing up to 100 times reduction in the inductor volume.

Figure 7. Hybrid boost converter results using a COTS vs. MEMS inductor.

3.3 Nanoparticle Self-assembly for MEMS Passives

While the high frequency circuits have leveraged on-chip MIM capacitors, MEMS capacitors could offer higher capacitance density and voltage handling (potentially for use as decoupling capacitors). However, such devices are often material and fabrication limited when integrating with CMOS circuits. Thus, we have developed a single chip, multi-material integration technique based on a well and capillary system. Nanoparticles, suspended in a liquid solvent, are delivered to the well and, subsequently, capillary action fills the channel with suspension. Once the capillary channel is dosed with suspension, evaporation driven assembly of the nanoparticles deliver ~100% of the suspended material to the channel (Bedair, 2009a). The vision for this room-temperature materials integration technique is an array of well and capillary structures. Each capillary is designed for delivery of either high-k dielectric nanoparticles for integrated capacitor fabrication or low loss, high frequency ferromagnetic nanoparticles for inductor fabrication (Bedair, 2010a).
The well and capillary channel were fabricated using the same copper electroplating process described in section 3.2. Nickel-ferrite nanoparticles (30 nm), suspended in methanol, were transferred to a channel with length, height, and width of 2 mm, 15 µm, and 10 µm, respectively. Models similar to “coffee” ring formation were then developed and showed excellent agreement with experiments (Bedair, 2010a). Figure 8 shows the liquid/solidified nanoparticles phase transition location, $L_T$, as a function of time, where $t = 0$ is the time the suspension is initially loaded into the channel through capillary forces. In figure 8, $L_T$ is scaled by the channel length, $L_c$.

![Figure 8](image_url)

Figure 8. (Top) Phase transition front (suspension/solidified nanoparticle region) compared to theory, and (bottom) copper microchannel channel before and after nanoparticle deposition.

Magnetization measurements (by an alternating gradient magnetometer, courtesy of Dr. Greg Fischer) were taken for the channel, which was sectioned from the well using a dicing saw. These measurements show a permeability of 3.3 and a volumetric packing density of 0.18, which compares with the 0.17 volumetric packing density as provided by the nanoparticle manufacturer (MTI Corporation). In other words, this technique shows packing densities similar to that achieved in the bulk case. We have used this technique to demonstrate both enhanced capacitors and inductors by depositing dielectric or magnetic nanoparticles, respectively (Bedair, 2011). The devices show improved performance far past 100 MHz, indicating the potential of this low-cost, room-temperature technique for developing high density power converters on a CMOS backbone (figure 9).
3.4 Piezo-MEMS Transformers

As an alternate to the magnetic and capacitive energy storage elements described previously, piezoelectric mechanical transformers are also being explored. In principle, the indirect piezoelectric effect is used to drive (via the input port illustrated in figure 10) the device into mechanical resonance, while the direct piezoelectric effect (output port) delivers power to a resistive load. Low frequency, bulk piezoelectric resonant transformers (< 5 MHz) have been implemented in power conditioning units in the past due to several advantages over magnetic core transformers including high voltage isolation, small size, and the absence of induced electromagnetic noise (Ivensky, 2004). At the smaller size scales, however, thin-film piezoelectric-transformer (PT) models and initial measurements show performances comparable with their larger (>4 mm²) SoA thin-film magnetic transformer counterparts (in the literature) at similar switching frequencies which suffer magnetic losses at high frequencies (Bedair, 2009b; Bedair, 2010b).

![Figure 10. Illustration of thin-film piezoelectric lead zirconate titanate (PZT) transformers: (left) the fundamental, n = 1, and (right) the third order length extensional device designs.](image-url)
Multiple generations of 1:1 PT devices were designed and tested (in collaboration with Jeffrey Pulskamp and Ronald Polcawich of the PZT MEMS group at ARL) and further proved enhanced performance at lower resistive, higher power loads. With fixed operating frequencies (~19 MHz), higher order length extensional modes (n = 3, 5, 9, and 13) were designed. The device lengths were 600 µm, 1 mm, 1.8 mm, and 2.6 mm, respectively. The devices’ widths and thicknesses were 40 and ~11 µm, respectively. The first and third mode devices are illustrated in figure 10. The RF performance was extracted from the frequency response using scattering parameter testing (figure 11). From the tests, motional resistance values, $R_m$, of 460, 316, 136, and 133 Ω were extracted for the respective modes. The impedance matched case for peak efficiency may then be predicted from the efficiency equation, $\eta = \frac{R_L''}{R_L'' + R_m}$, where $R_L''$ is the real part of the reactive load. The predicted impedance matched resistive loads, $R_L$, are 700, 350, 180, and 120 Ω, respectively. Based on the reactance of the output port for these designs, the respective efficiencies are predicted to be 45%, 36%, 40%, and 30%.

This testing has confirmed our initial modeling efforts predicting that tailoring the geometry and the input and output electrode coverage provides a means to impedance match to various electrical loads, which in a power converter directly affects efficiency, the voltage buck/boost ratio, and power delivery. These efficiencies compare with thin-film magnetic transformers at similar loads and switching frequencies in the literature; however, the areas occupied by the PTs are 10–100 times smaller than those in the literature. Power densities >10 W / mm$^3$ were measured and confirmed with PZT-on-silicon structures. However, further measurements are required to accurately characterize the power handling of each device at higher power levels, as we are currently limited by the measurement instrument’s maximum output power. With such miniature scales in size and similar performance to the magnetic case, these transformers offer a viable, alternate approach to ultra-compact, high frequency solution for power converters. With each PT occupying a total volume in the hundreds of cubic micrometers, a power unit composed
of an array of impedance matched PTs is envisioned as a potential ultra-miniature power conditioning unit capable of adapting to a variety of loads.

4. Conclusions

4.1 Transitions

By initiating research that addresses the often ignored gap between the source and load of small systems, numerous opportunities for collaboration and transition across the Department of Defense (DoD) have been identified that can leverage the size, speed, or power density of our converter research. From the absolute size scales we initially targeted, the MAST CTA is an obvious first choice. Collaborations with Prof. Rob Wood (Harvard) on powering his micro-robotic fly have begun, as our circuits could serve as an enabling technology for achieving self-contained lift on his previously tethered platforms. Tagging, tracking, and locating (TTL) and small unattended ground sensors (UGSs) are other obvious size-constrained applications where the size and ability of our converters to be co-designed in a single CMOS process with other application-specific integrated circuits (ASICs) is attractive. The speed of our converters also offers potential benefits for mesoscale systems like ARL’s Blue Radio program, which currently has in-rush current problems due to the slow nature of their power converters; slight adaptation of our technology could minimize this parasitic power draw and improve mission lifetime considerably. Similarly, missile health monitoring units (HMUs) being developed by the Army Missile Research, Development and Engineering Center (AMRDEC) must power multiple subsystems with low average power draws and converters offering fast response and low overhead can substantially affect system longevity. Primary power supplies in compact missiles also require multiple voltage levels simultaneously but with power draws in the watts to tens of watts range. As a result, COTS solutions add a large parasitic weight and inefficiency to the missile’s electronics package, reducing volume available for inertial measurement units (IMUs) or other components, which can affect accuracy and/or control authority of the missile flight—yet another opportunity for faster converters with higher power density to offer improved system performance. Finally, some of the technology developed in this program has received significant attention from outside organizations for spin-off applications, such as the Armament Research, Development and Engineering Center (ARDEC), who would like to explore using our nanoparticle wicking technique to make multi-material fire trains for miniature fuzes in munitions.

4.2 Future Research

While progress to this point has been tremendous, significant research remains in all of the areas outlined previously. Fully integrating the CMOS circuits and MEMS passives into a standalone converter will require packaging and integration details to be addressed. Expanding our work to
demonstrate multiple inputs and outputs, as well as extending our circuit techniques to higher voltage CMOS processes, should enable significantly higher power densities across a wide range of applications. In addition to microscale fuzes, the base processes developed for MEMS inductors and capacitors are being modified to further improve performance, but will also be investigated to enable new devices like dynamic inductors for tuning in RF systems, or perhaps as antenna balun transformers. Finally, the PT thrust is an exciting new paradigm in compact converters that potentially offers superior size scales and/or power density, but it remains unproven at the circuit level, which therefore will be a focus going forward.
5. References


# List of Symbols, Abbreviations, and Acronyms (required if more than 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>AMRDEC</td>
<td>Army Missile Research, Development and Engineering Center</td>
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<td>ARDEC</td>
<td>Armament Research, Development and Engineering Center</td>
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<td>ARL</td>
<td>U.S. Army Research Laboratory</td>
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<tr>
<td>ASIC</td>
<td>application-specific integrated circuit</td>
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<td>CMOS</td>
<td>complementary metal oxide semiconductor</td>
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<td>COTS</td>
<td>commercial off the shelf</td>
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<td>CTA</td>
<td>Collaborative Technology Alliance</td>
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<td>DoD</td>
<td>Department of Defense</td>
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<td>HMUs</td>
<td>health monitoring units</td>
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<td>IMUs</td>
<td>inertial measurement units</td>
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<td>LiPo</td>
<td>lithium polymer</td>
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<td>MAST</td>
<td>Micro Autonomous Systems and Technology</td>
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<td>MEMS</td>
<td>micro-electromechanical systems</td>
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<td>MIM</td>
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<td>negative metal oxide semiconductor</td>
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<td>PWM</td>
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<td>RF</td>
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<td>SC</td>
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<td>SoA</td>
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<td>7 HCS</td>
<td>US ARMY RSRCH LAB ATTN RDRL SER JOE MAIT ATTN RDRL SER L BRETT PIEKARSKI GABE SMITH WILLIAM NOTHWANG ATTN RDRL SED E PAUL BARNES BRUCE GEIL ATTN RDRL SES P GREG FISHER ADELPHI MD 20783-1197</td>
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