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Gallium Nitride (GaN) High Power Electronics (FY11)

by Kenneth A. Jones, Randy P. Tompkins, Michael A. Derenge, Kevin W. Kirchner, Iskander G. Batyrev, and Shuai Zhou

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14. ABSTRACT

This report covers work done for the Director's Research Initiative (DSI) on Gallium Nitride (GaN) High Power Electronics (HPE) in which GaN devices are assessed in comparison to those fabricated from silicon carbide (SiC). We show that for low power applications (< 1500 V) GaN diodes should have a lower on-resistance, and therefore less loss, than their SiC counterparts because the critical breakdown field and electron mobility are larger. We expect this will also be true for HPE GaN high electron mobility transistors (HEMTs) compared to SiC metal-oxide-semiconductor field effect transistors (MOSFETs). Although a few GaN devices have been made that have properties that exceed those made from SiC, these devices cannot yet be manufactured. Our work suggests the dominant problem is contamination of the metal-organic chemical vapor deposition (MOCVD) films by the carbon in the trimethyl gallium (TMGa). We suggest a better alternative is to grow the films by hydride vapor phase epitaxy (HVPE), which requires that conducting GaN substrates be grown to reduce the on-resistance ($R_{ON \cdot SP}$) for the back side diodes. We also show that dislocations appear to strongly affect diode properties such as the ideality factor, but their effect on the breakdown voltage appears to be a less significant problem than was previously thought.

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1. Introduction

1.1 Rationale

Gallium nitride (GaN) high power electronic (HPE) devices have the potential to outperform those made from 4H-silicon carbide (SiC), the polytype used for HPE devices, because it has a larger critical electric field, ξ_C, the field at which the device breaks down –3.5 versus 2.5 MV/cm. This is primarily due to the fact that it has a larger energy gap, E_G – 3.39 eV versus 3.25 eV. It also has a larger electron mobility, μ – 1245 versus 1000 $cm^2/V\cdot s$. This enables GaN to theoretically have better device properties. One of them is the minimum thickness for the device, which is the width of the depletion layer when the device breaks down, W_B, so that the depletion layer will not "punch through" the device before it breaks down. Thus,

$$W_B = 2V_B/\xi_C, \tag{1}$$

where V_B is the breakdown voltage. The maximum doping level in the drift region, n_{dmx} α W_B^2, so

$$n_{dmx} = (\varepsilon\xi_C^2)/(2qV_B), \tag{2}$$

where ε is the electric permittivity. Thus, GaN can be more heavily doped. Combined with the higher mobility, this enables GaN to have a smaller specific on-resistance, $R_{ON\cdot SP}$, for a given V_B, where

$$R_{ON\cdot SP} = 4V_B^2/\mu\varepsilon\xi_C^3. \tag{3}$$

This is one of the most important parameters because it determines the loss when the device is turned on. As a result, the figure of merit (FOM) is defined to be

$$FOM = V_B^2/ R_{ON\cdot SP} \tag{4}$$

and it is illustrated in the theoretical plot of $R_{ON\cdot SP}$ versus V_B in figure 1, along with some of the better experimental values. Note that the experimental value recently achieved by the Japanese (*1*) exceeds the theoretical value for 4H-SiC even though it was achieved using a relatively poor GaN substrate containing $>10^6$ dislocations/cm^2. The relative FOM (RFOM) is the ratio of the FOMs for a given material, and the value for GaN shown in table 1 is 3.3 times larger than it is for 4H-SiC even though the ratio of the critical fields is only 1.4 primarily because $R_{ON\cdot SP}$ α ξ_C^{-3}.

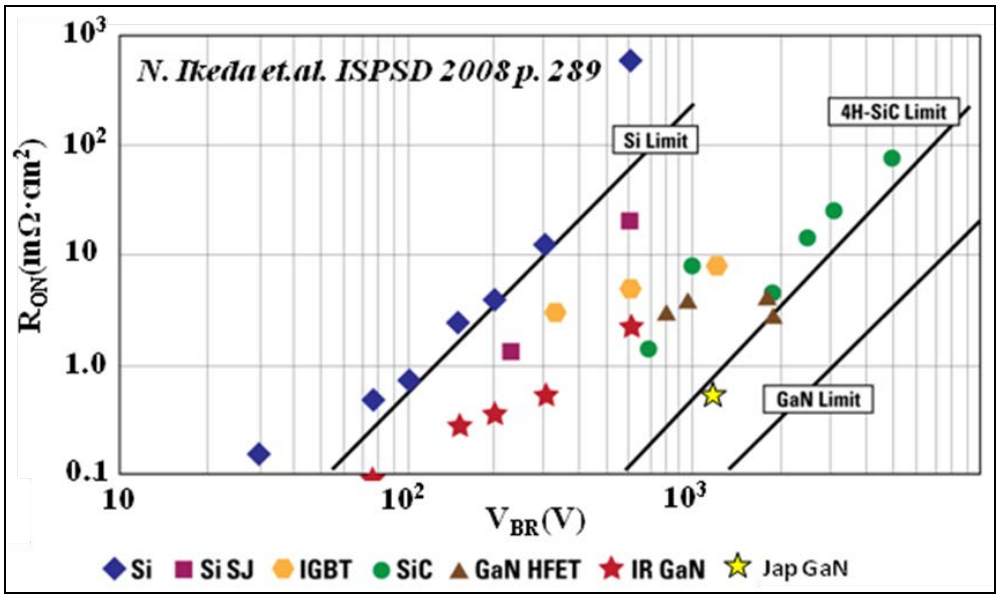

Figure 1. Plot of the theoretical specific on-resistance as a function of the breakdown voltage for silicon (Si), SiC and GaN, along with experimental values that have been obtained by a number of researchers.

Table 1. Values for some physical parameters for Si, 4H-SiC, and GaN.

	Si	SiC	GaN
$\varepsilon/\varepsilon_o$	11.8	9.7	9.5
μ_n(cm²/V·s)	1400	1000	1245
ξ_C (V/cm)	.25 x 10^6	2.5 x 10^6	3.5 x 10^6
W_B (μm)	80	8.0	5.7
n_d (cm^{-3})	2.0 x 10^{14}	1.9 x 10^{16}	3.2 x 10^{16}
$R_{on\cdot sp}$(mΩ/cm²)	173	0.30	0.09
RFOM		582	1925

Another advantage GaN has is that it can form solid solutions with other Group III elements such as aluminum (Al) to form aluminum gallium nitride (AlGaN). The energy gap increases with the Al concentration, as does ξ_C, suggesting that AlGaN might be the HPE semiconductor material of the future following SiC/GaN. The ability to form a solid solution also increases the diversity of the devices one can fabricate. An important one is the high electron mobility transistor (HEMT) in which a two-dimensional electron gas (2DEG) with an electron mobility that can be more than twice what it is in the bulk is created at the AlGaN/GaN interface. It is larger because the electrons are supplied by donors in the AlGaN that are separated from the 2DEG so they do not as effectively scatter them. Also, the AlGaN/GaN interface can be very smooth because the AlGaN grows epitaxially on the GaN and does not contain mismatch dislocations when its

thickness is less than its critical thickness. This high mobility, which can be as large as 2500 $cm^2/V \cdot s$, can lead to a small channel resistance, the resistance that can dominate $R_{ON \cdot SP}$ for a transistor for $V_B < 3000$ V.

In contrast, SiC is a compound with a fixed composition. Second phases are formed, as opposed to solid solutions, when the Group IV elements, carbon (C), Si, or germanium (Ge) are added to it. In order to form a 2DEG, a dielectric, usually silicon dioxide (SiO_2), has to be grown or deposited on the SiC. This complex interface contains many defects and can be rough especially if the oxide is grown, as it usually is. These attributes, as well as others, have so far limited the channel mobility to ~25 $cm^2/V \cdot s$. This has caused the channel resistance to be the dominant resistance for $R_{ON \cdot SP}$ in the SiC metal-oxide-semiconductor field effect transistors (MOSFETs) that are currently being used.

Another advantage is that the dominant crystal structure for GaN is the hexagonal 2H structure. The cubic 3C structure has been seen in stacking faults near the hetero-interface between the GaN film and the substrate it is growing on caused by the mismatch between them, but this phase is not nearly as stable as the 2H phase. There is also no evidence that applying a large current will alter the 2H phase. On the other hand, SiC has ~250 phases—sometimes called polytypes—of which the most common are the 3C, 4H, and 6H polytypes. These structures differ only in how their close packed basal planes are stacked on top of each other. 3C is said to have an AαBβCγAα…, 4H an AαBβAαCγAα… and 6H an AαBβCγAαCγBβAα… structure, where the Latin letter represents Si atoms and the Greek letters represent C atoms. The 4H structure is the desired structure for HPE electronics, and it has been shown that when large electrical currents are passed through it, the 4H structure is converted into 3C in some regions, and the associated stacking faults cause the on-resistance to increase with time (*2*). This problem can be minimized by greatly reducing the concentration of basal plane dislocations that catalyze the transformation from 4H → 3C, but this process is expensive.

Finally, more money is being invested into GaN than any other semiconductor except Si because of the great interest in blue/ultraviolet (UV) emitters and detectors and higher power radio frequency (RF) HEMTs. These considerable investments can be leveraged for GaN HPE. Some people are concerned about the relative scarcity of gallium (Ga), but to date this has not been a problem.

1.2 Challenges

GaN device structures contain a large number of defects. One type is structural defects, most of which are dislocations created by the mismatch between the GaN film and the substrate it is grown on. The structure is a heterostructure—that is, the film and substrate are different materials—and the difference in their lattice parameters is accommodated by the formation of misfit dislocations. Hetero-substrates are required because, until very recently, large, good quality GaN crystals have not been grown. They cannot be grown in the traditional manner because GaN sublimates at normal pressures, and the nitrogen (N_2) partial pressure in

equilibrium with the GaN is extraordinarily high at reasonable growth pressures (*3*). As a result the GaN films are grown primarily on (0001) oriented sapphire (Al_2O_3), which has a 13% mismatch, or (0001) SiC, which has a 3.5% mismatch. Even though the dislocation concentration is larger at the film/substrate interface, a large number of dislocations, called threading dislocations propagate through the film. Typically, there are ~10^9 threading dislocations/cm^2 in the GaN films grown by metal-organic chemical vapor deposition (MOCVD) and ~10^{10} in films grown by molecular beam epitaxy (MBE) when they are deposited on either one of these substrates.

Another type of defect is point defects, many of which are electrically active; they can be n- or p-type dopants or hole or electron traps and they usually act as scattering centers that reduce the carrier mobility. They are introduced in a controlled manner when the GaN is deliberately doped, but they are also introduced unintentionally by impurities in the system, such as Si, oxygen (O), and C. It is generally agreed that Si and O are shallow donors (*4*). There is some disagreement about C, as some believe it sits on a N site and is a deep acceptor acting as an electron trap (*5*), others have suggested that it sits on a Ga site, where it acts as an acceptor (*6*), and it has also been pointed out that it could be an interstitial (*7*). Calculations show that under equilibrium conditions the C atom is likely to occupy an N site when the material is n-type and acts as an electron trap, but film growth is a kinetically controlled process, so it is likely that at the end of the growth, the C atoms occupy all three types of sites. N vacancies and interstitials are also believed to be electrically active with the vacancy acting as a shallow donor (*8*), and the interstitial acting as an acceptor (*9*); the vacancy is believed to be much more stable. Ga vacancies also exist, and they are believed to be electron traps (*10*). Individual point defects can also combine to form more complex structures, such as a Ga vacancy bound to an O donor (*11*), that are also electrically active. The number of possibilities is large, and it is a challenge to determine which property is related to which defect(s).

The challenges are to determine which type of defect—line or point—has the most pronounced negative effects on the operation of high power Schottky diodes, (SDs) and then which line or point defect is the most detrimental. The next step is to determine ways to eliminate them or at least mitigate their negative effects.

2. Approach

To determine the effect of dislocations on the properties of the diodes, the films grown by MOCVD were deposited with an (0001) orientation on different substrates, which resulted in a different number of dislocations being formed in the films. One substrate was sapphire, and the film grown on it was expected to have ~5 x 10^9 dislocations/cm^2, because the lattice mismatch between the GaN film and the sapphire substrate is very large—13.8% (*12*). Another substrate was a free-standing GaN substrate that was created by growing a film a few millimeters thick on

a sapphire substrate using the hydride vapor phase epitaxy (HVPE) technique, and then removing the substrate by rapidly heating it with laser light that is transparent to the sapphire, but is absorbed by the GaN. This substrate, L-HVPE, contains fewer dislocations—~5 x 10^6/cm^2—because some of the dislocations created near the film-substrate interface grow out of the film. The HVPE (*13*) technique is used because the growth rate can be as high as 200 μm/h, which is ~200 times faster than the MOCVD growth rate. One of the substrates, H-HVPE, is doped to reduce the substrate resistance, but fewer dislocations grow out of the film so it contains ~5 x 10^7/cm^2. The fourth substrate is a GaN substrate grown by a newly developed ammono-thermal process, and it contains only ~5 x 10^3/cm^2 (*14*).

The primary dislocations that are created in (0001) GaN films are threading edge (TE) (sometimes called *a*), screw (sometimes called *c*), and mixed (sometimes called *c* + *a*) (*15*). They can be identified nondestructively using electron channeling contrast imaging (ECCI) (*16*). "Good" and "bad" diodes were identified by their electrical measurements, and then the Schottky metal was etched off, and the dislocations that lay under it were identified. An attempt was made to correlate the number and type of dislocation with the electrical properties.

The number and type of point defects are controlled by the cleanliness of the environment, the growth pressure, P, and the growth temperature, T. The environment is affected by the growth methods that you use, which in our case are the MOCVD and HVPE methods shown in figure 2. In the MOCVD method a source of C is the methyl groups on trimethyl gallium (TMGa). Whereas the methyls do not appear to be a C source in the MOCVD growth of GaAs, it is more likely that they are in the growth of GaN because it is grown at a significantly higher T—~1050 ºC versus ~600 ºC. Higher temperatures are required because the H is more strongly bonded to the N in ammonia (NH_3) than it is bonded to the arsenic (As) in arsine (AsH_3). In addition, the NH_3 is not generally as pure as the AsH_3 because purity in GaN is not yet as important an issue as it is for gallium arsenide (GaAs). The two other primary chemical contaminants found in MOCVD grown GaN are Si and O (*17*), but it is not clear what the sources are. For HVPE GaN films the C level is below the detection limit of ~10^{16} cm^{-3}, and the Si and O levels are >10^{16} cm^{-3} (*18*). These numbers are discouraging for high voltage devices since for V_B > 3 KV, the doping levels should be in the mid to lower 10^{15} cm^{-3} range. However, since the focus of this work is to create devices with V_B > 600 V, which are required for hybrid electric vehicles, this appears not to be an important issue at this time.

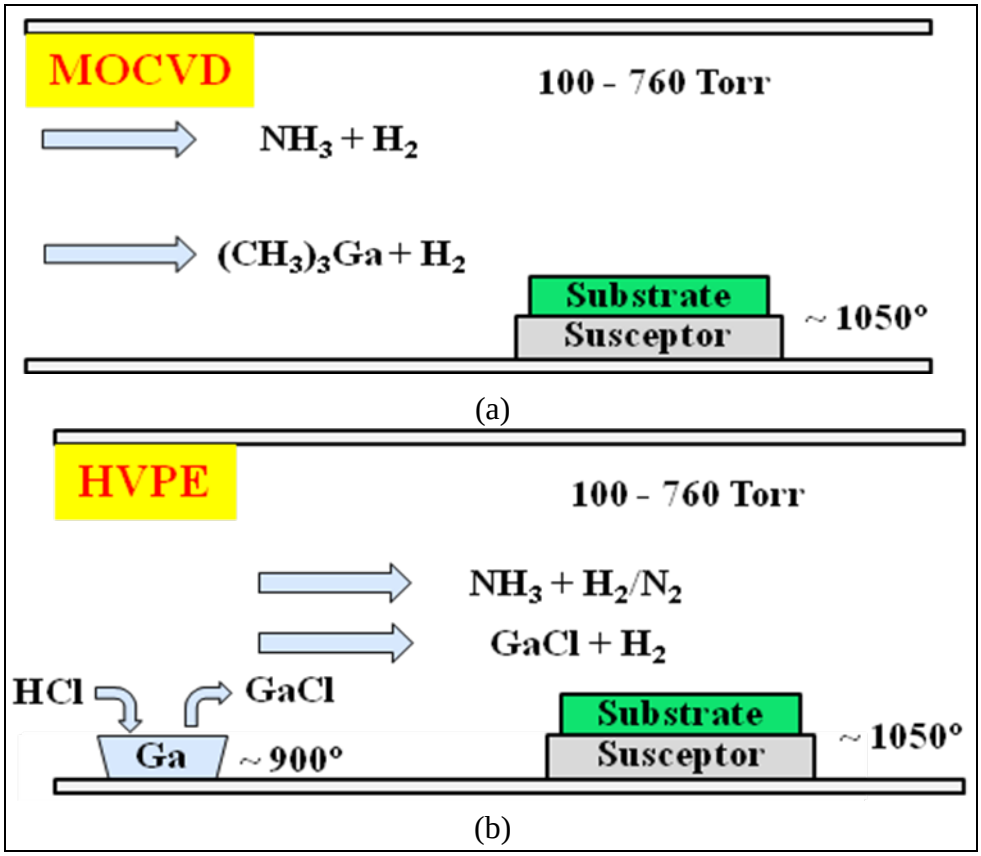

Figure 2. Schematics of the (a) MOCVD and (b) HVPE growth systems used to grow the SD device structures.

The SD device structure for examining the effects of dislocations on the properties of the devices was simply a 3 μm n^+ layer doped to ~10^{19} cm^{-3} followed by an unintentionally doped (UID) layer 5 μm thick. The films were grown by MOCVD at T = 1000 °C and P = 500 Torr with the V/III = NH_3/TMGa = 3500. The GaN substrates were 1 cm on a side, and the sapphire substrate was a quarter of a 2" sapphire wafer. For the structure grown on the sapphire wafer a template composed of a 2 μm UID GaN film deposited on the wafer was used so that all of the device structures could be grown simultaneously. X-ray rocking curves (RCs) were taken of the substrates prior to and after film growth. Both the symmetric (0002) and asymmetric (10$\underline{1}$2) peaks were used. The former measures lattice rotations produced by the dislocations about an axis in the growth plane, and the latter measures rotations about an axis perpendicular to it.

The diodes fabricated on a sapphire substrate were front-side diodes because it is an insulator; the other three sets of diodes were back-side diodes, which have the ohmic contact on the back side as is shown in figure 3. In both cases, the ohmic contact was formed by a titanium (Ti)/Al/nickel (Ni)/gold (Au) (250/2200/600/500 Å) stack that was annealed in N_2 at a temperature of 750 °C for 30 s. The Schottky contacts were formed by a Ni/Au (500/1500 Å) bilayer after a SiN_x layer had been deposited by plasma enhanced chemical vapor deposition (PECVD). It was used for edge termination as it extended ~10 μm in under the metal contact.

The mesas for the front-side diodes were fabricated using a chromium (Cr)/Ni mask and an inductively coupled plasma (ICP) boron tricholride (BCl_3)/chlorine (CL_2)/argon (Ar) etch.

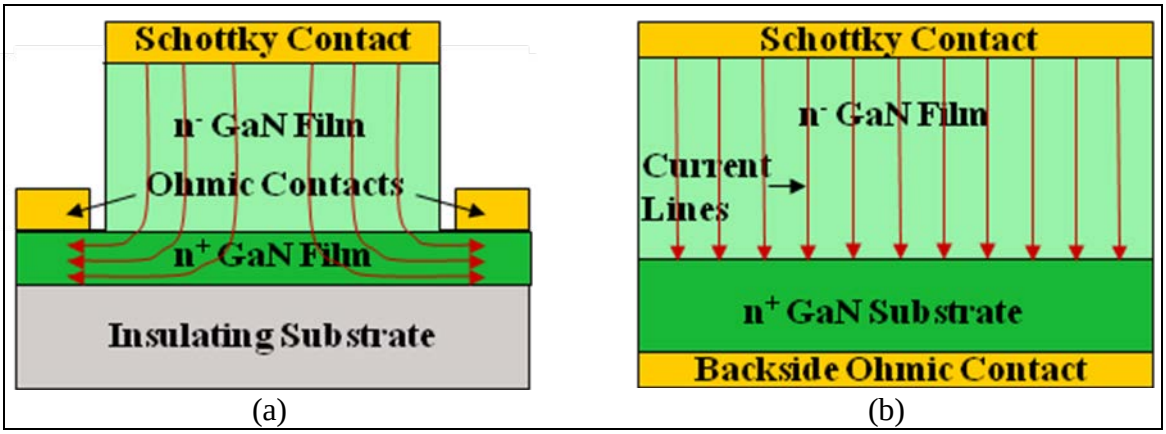

Figure 3. Schematic diagrams of SDs with (a) front-side contacts and an insulating substrate, and (b) backside contacts and a conducting substrate.

The diode diameters vary in size from 30–300 μm and in number as shown in the cell layout in figure 4a, and the step and repeat cell pattern is displayed in figure 4b. Capacitance-voltage (C-V) measurements were performed to determine the net carrier concentration. Current-voltage (I-V) characteristics were measured in a probe station using both a semiconductor parameter analyzer for forward voltages and reverse voltages to 100 V, and a curve tracer for reverse voltages >100 V. Parameters such as the turn-on voltage, V_{ON}, defined as corresponding to the voltage at which the forward current density is 100 A/cm^2, ideality factor, *n*, barrier height, φ, $R_{SP\cdot ON}$, and V_B were extracted from the forward and reverse I-V curves using standard linear curve fitting techniques to the diode equation.

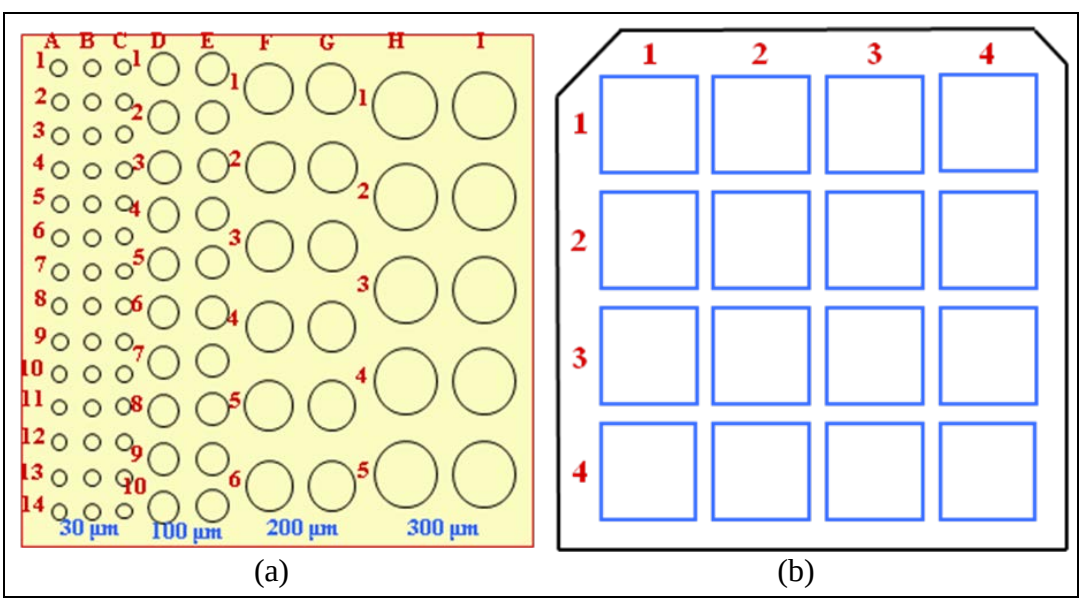

Figure 4. (a) Layout of the diodes in a unit cell and (b) layout of the cells on ~1 cm x 1 cm wafer.

Front-side diodes have the advantages that they have no substrate resistance, R_{SUB}, and they can be used in integrated circuits, and the disadvantages are that they require deep etches, and current crowding occurs near the ohmic contacts. Things are reversed for the back-side diodes, as the advantages are that no mesa etch is required, and there is no current crowding at the ohmic contact. However, they do have a R_{SUB}, and they cannot be used in integrated circuits.

After the electrical measurements had been made, the Schottky metal was stripped off some of the diodes with a selective etch, and the surface that was under the metal was examined using ECCI to determine the type and number of dislocations that were in the active GaN layer under the metal. Diodes with "good" characteristics were compared with those that had "bad." Diodes with 10 μm diameters had to be fabricated to insure there would be some diodes with no dislocations under them, and others would have only threading edge dislocations beneath them, while others would have only dislocations with a screw component. Also, the C, O, Si, and H impurity concentrations were measured for some of the diodes using secondary ion mass spectroscopy (SIMS) to determine if the structural quality of the film affected the incorporation of the impurities.

In addition to using the SIMS measurements to study the effects of point defects on the device properties, we fabricated both front- and back-side SDs on low doped HVPE substrates without growing a film on them. We were able to grow a few HVPE films on ammono-thermal and HVPE substrates, but this effort was greatly limited because Kyma Technologies, who did the HVPE growth, has not yet received their Phase II Small Business Innovative Research (SBIR) funds even though the contract was awarded in January 2011, because the Defense Contract Audit Agency (DCAA) had an issue with Kyma's accounting system and has not been helpful in assisting Kyma to rectify the problem.

3. Results

3.1 Effects of Crystalline Defects

The symmetric and asymmetric rocking curves for the films with the four different types of substrates are shown in figure 5. The ammono-thermal film clearly has the highest quality, as the (0002) RC has a peak width of only 22″ and for the $(10\underline{1}2)$ it is only 26″. They are only a few arcsecs larger than they were for the substrate. The film on the low doped HVPE substrate has wider RCs – especially the $(10\underline{1}2)$ peak, which is 231″ wide compared to a width of 53" for the (0002) peak. Interestingly, the asymmetric peak width for the substrate, 55″, was much less, whereas the symmetric peak width, 86″, was larger than it was for the film. The film grown on the higher doped HVPE substrate, H-HVPE, clearly has poorer structural quality as it has a symmetric peak width of 167″ and an asymmetric peak width of 253″. However, the quality is superior to the film grown on the sapphire substrate, which has peak widths of 316″ and 447″.

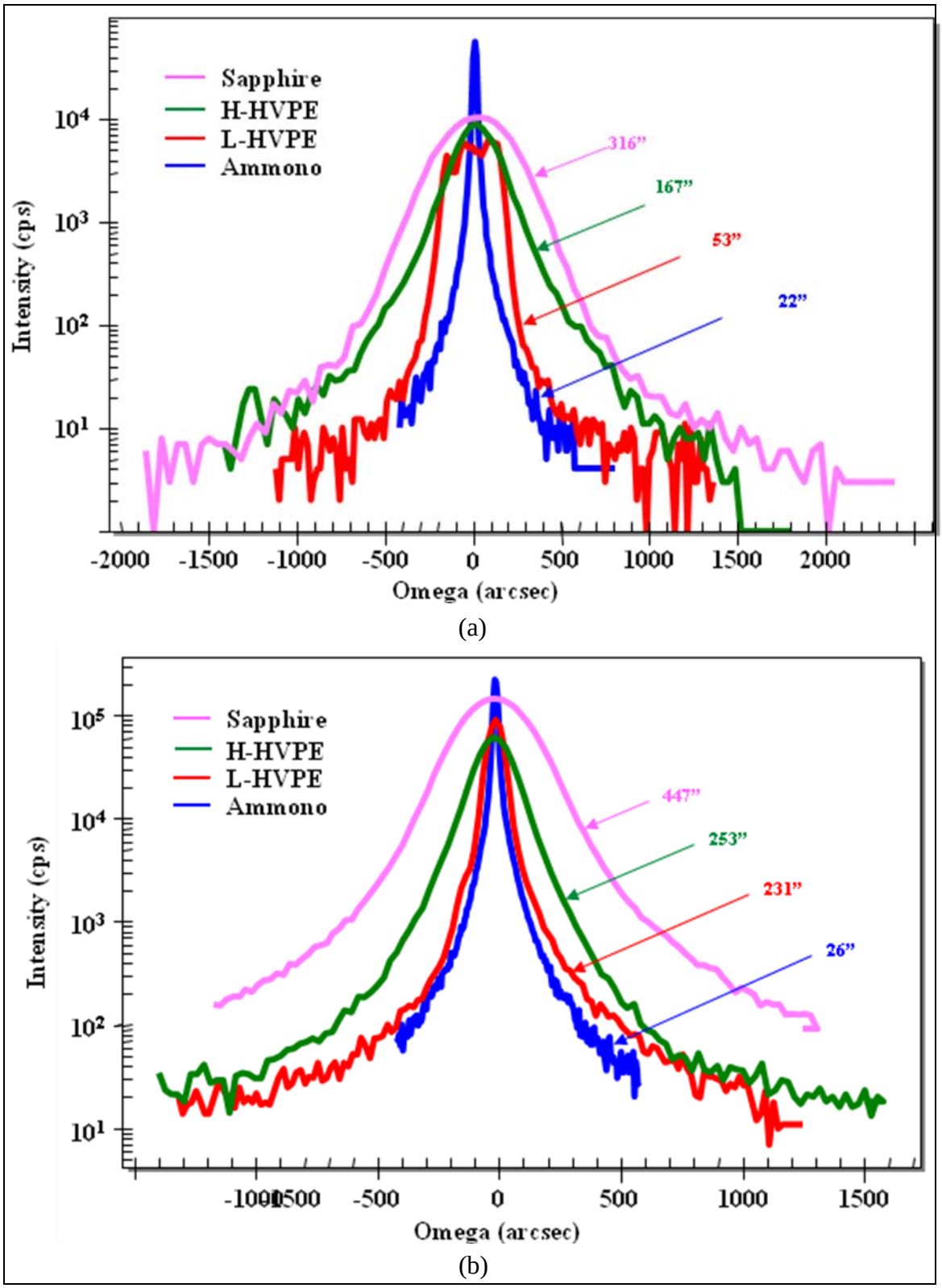

Figure 5. (a) Symmetric and (b) asymmetric rocking curves for the four samples with different dislocation concentrations.

The net carrier concentration for the films grown on the four different types of substrates was determined from the C-V curves in figure 6. They are within a factor of two of each other with the values being 1.39, 1.71, 1.06, and 1.95 x 10^{16} cm^{-3} for the ammono-thermal, L-HVPE, H-HVPE, and sapphire substrates, respectively. The median breakdown voltages for the diodes prepared on these samples that are shown in figure 7 are disappointingly low. This is especially true for the Ammono diodes because they were fabricated from films that had the best crystalline structure that has ever been prepared. This suggests that for these device structures, the types of point defects and their concentration played a more dominant role in determining the breakdown than the defect structure did. In the past we have attributed the wide variation in V_B across the wafer and the reduction of in its median value as the diameter of the diode increases to variations in the defect structure. One could argue that the variation is due to a variation in the point defect concentration caused by the variation in the defect structure, but then one would expect the variation to be smaller in the films grown on higher quality substrates to be less, and it is not, as shown in figure 8, where all of the breakdown voltages for each of the four diameters are plotted for the Ammono and L-HVPE samples. It also is not clear why the devices on the L-HVPE sample tend to have a larger V_B.

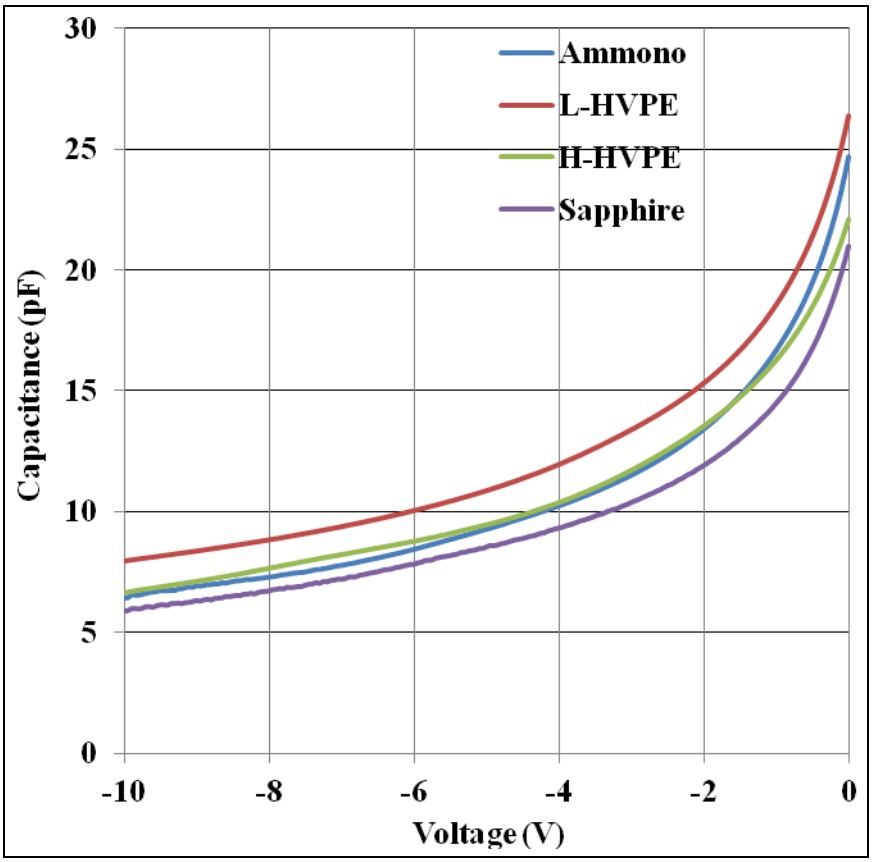

Figure 6. C-V curves for the films grown on the Ammono, L-HVPE, H-VPE, and sapphire substrates used to compute their net carrier concentrations.

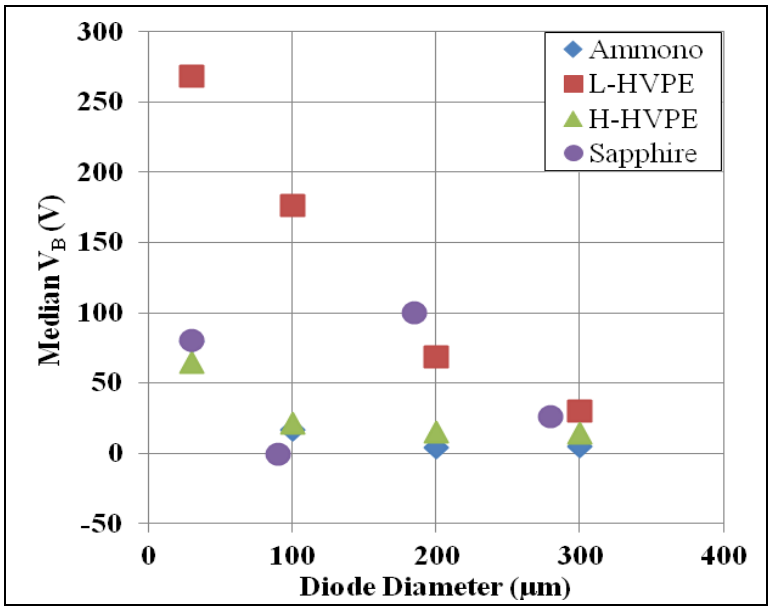

Figure 7. The median V_B for the Ammono, L-HVPE, H-VPE, and sapphire samples for the diodes with the four different diameters.

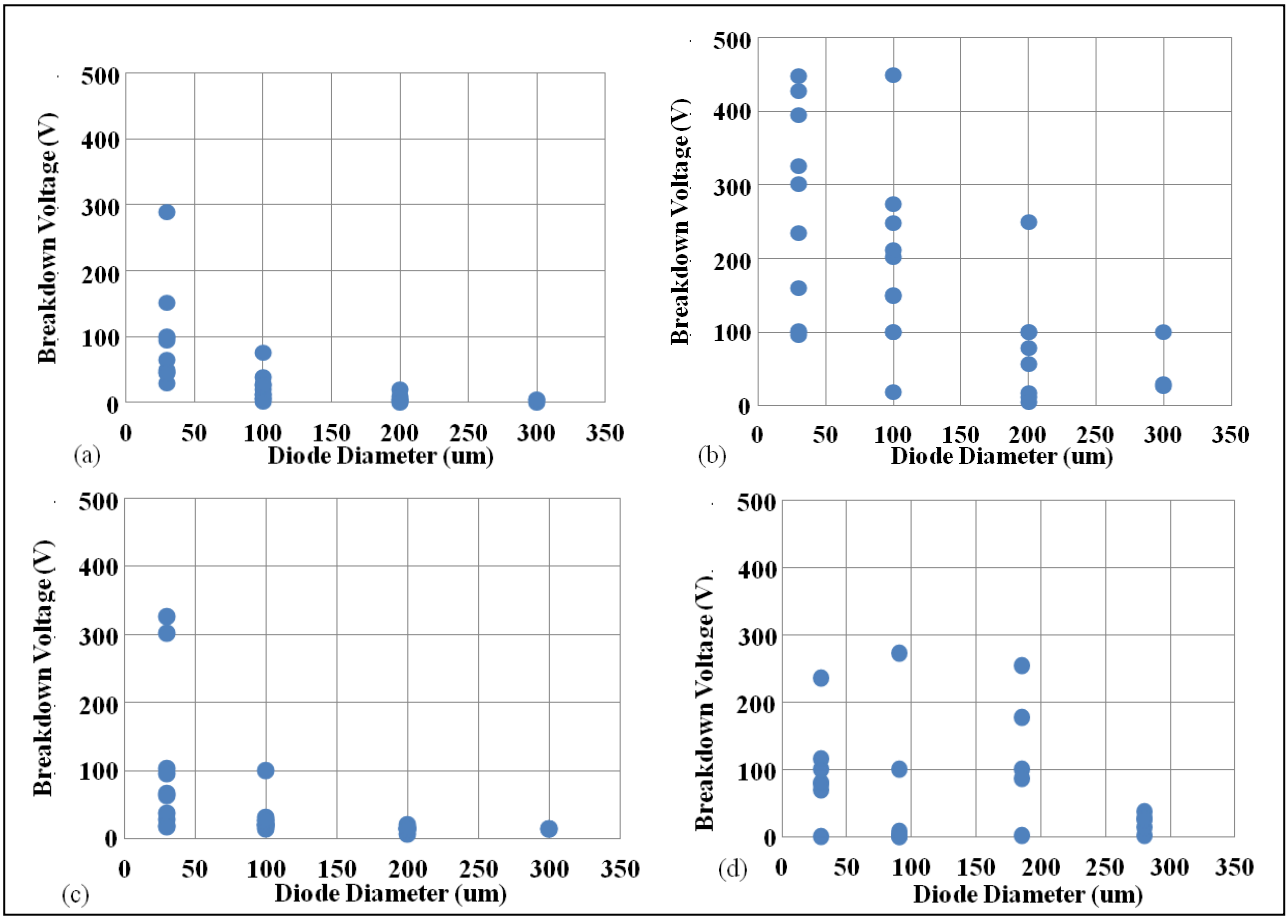

Figure 8. The V_B for the (a) Ammono, (b) L-HVPE, (c) H-VPE, and (d) sapphire samples plotted for each of their four diameters.

This is not to say that defects do not affect V_B and other device properties. Dislocations have strain fields that can be reduced by impurities preferentially diffusing to them, and the local increase in the dopant concentration will reduce the local V_B. However, the effects of dislocations are more profound (*19*). For example, it has been shown that the size of the energy gap changes in the vicinity of the dislocation, and if it is smaller, this would lower V_B (*20*). It is more likely that a dislocation creates defect states in the bandgap, and carriers in them are more easily ionized by the electric field than those in the valence or conduction band are. It has been qualitatively shown that defect states associated with dislocations increase the leakage current and lead to soft breakdowns, and those with a screw component are considered to be more detrimental (*19, 21*). It is clear that they do have an effect because diodes fabricated in the low dislocation region of lateral epitaxial overgrowth (LEO) films have smaller leakage currents and more ideal forward bias characteristics than those fabricated in the high dislocation region (*22*). It is just that the point defects appear to have more dominant effects.

The ECCI (figure 9) done by Prof. Picard on the Army Research Office (ARO) SBIR and Technology Transfer Research (STTR) support the idea that dislocations did not play the dominant role in the lower than expected V_B. This can be seen in the V_B plotted as a function of the threading edge dislocation density and those with a screw component in figures 10a and b. The diodes were back-side diodes fabricated on an HVPE substrate. Diodes with no dislocations under them had very different V_B, and some with more than a single dislocation under them had $V_B > 600$ V.

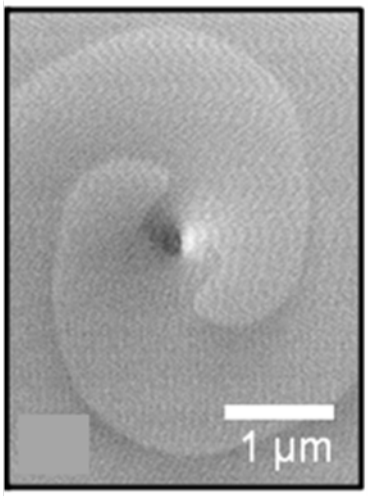

Figure 9. An ECCI image of a dislocation.

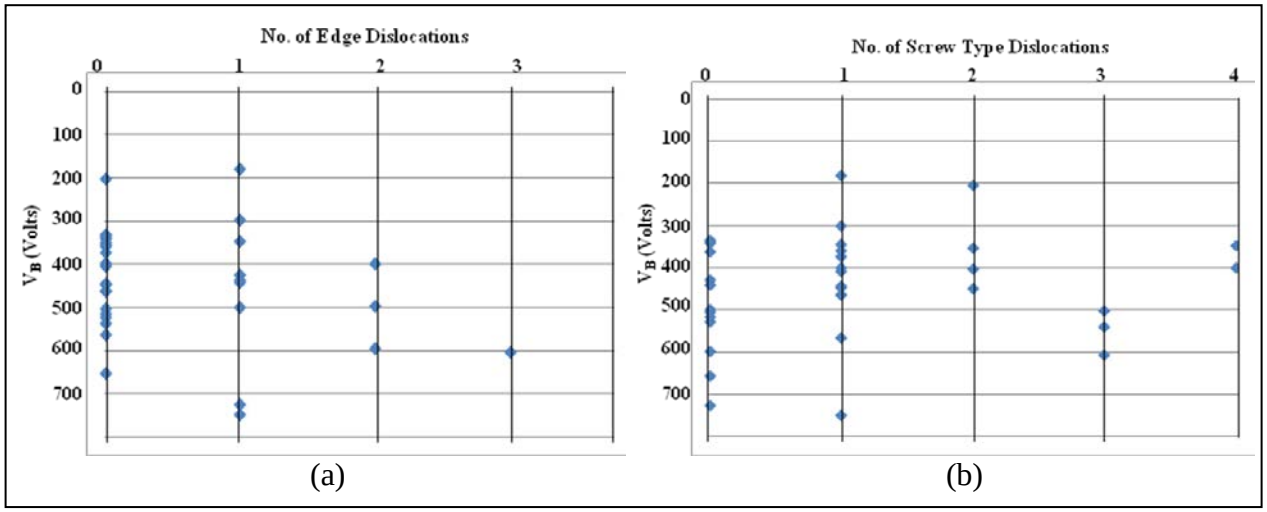

Figure 10. (a) V_B plotted as a function of the concentration of dislocations with a screw component and (b) as a function of threading edge dislocations.

3.2 Point Defects

The ideality factor versus the barrier height curves in figure 11 tell another story. The points are bunched around $n \sim 1.1$ and $\varphi \sim 0.80$ for the Ammono sample. The small n is indicative of fewer deep states in the energy gap (*23*) suggesting that dislocations might be a source of some of these states. It is not clear why φ is a little smaller than it is for the other samples. The average value of n for the L-HVPE sample increases compared to the Ammono SDs, it increases still more for the H-HVPE sample, and it is the largest for the SDs on the sapphire sample. As good as the parameters for the Ammono sample are, they are not as good as those for the backside SDs fabricated directly on a low doped hydride wafer last year, as is shown in its n versus φ plot in figure 11. Note that the axes have different scales, and that many of the diodes have n values between 1.00 and 1.10, as well as φ values between 0.80 and 0.90. This suggests that the point defects associated with the small V_B is related to carbon since the HVPE material does not have an obvious source of it.

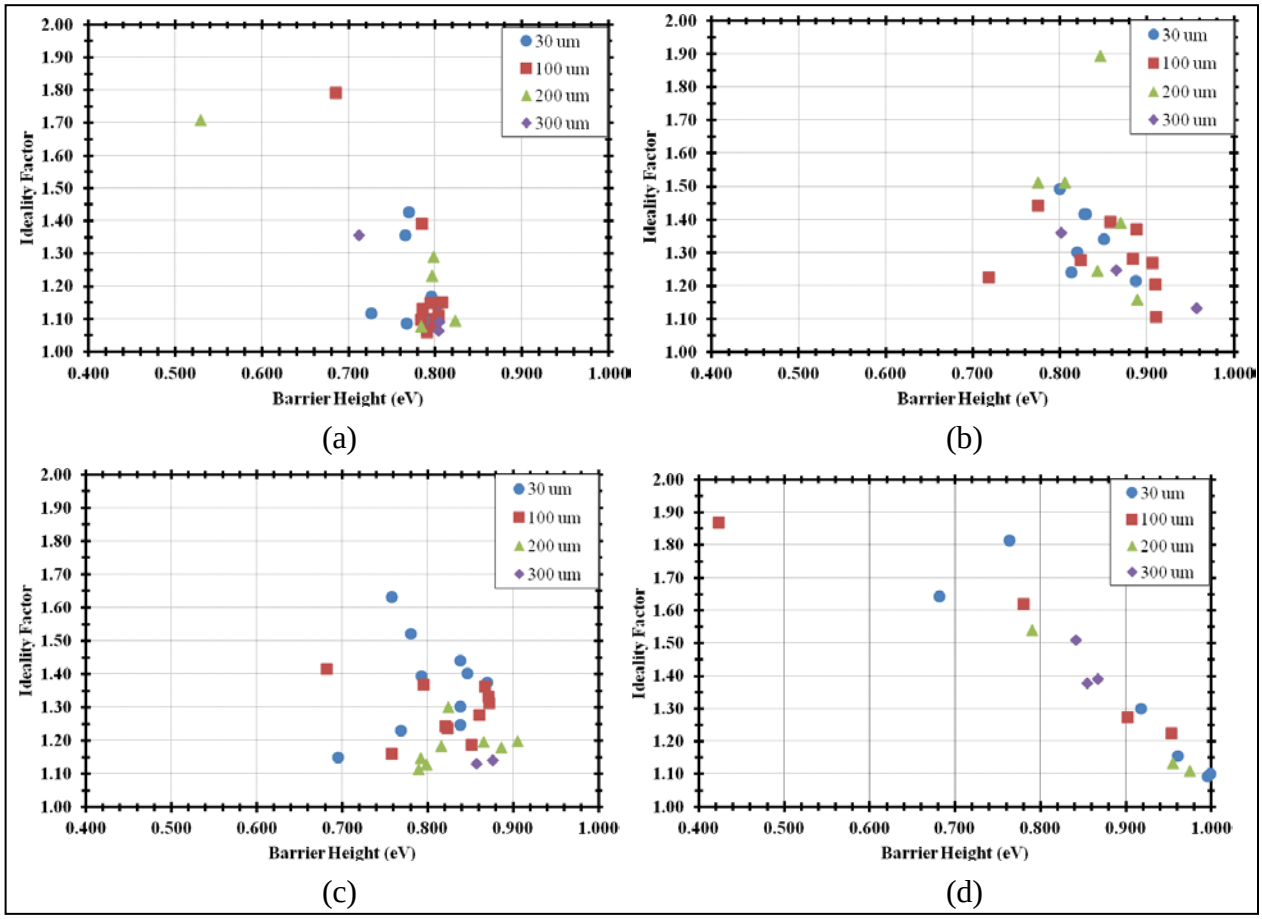

Figure 11. *n* vs φ curves for SDs on the (a) Ammono, (b) L-HVPE, (c) H-HVPE, and (d) sapphire wafers.

The SIMS data in figure 13 show that all of the samples have a substantial amount of carbon in them varying from 5 x 10^{16} cm^{-3} for the sapphire sample to 1 x 10^{17} cm^{-3} for the H-HVPE sample. With the exception of the sapphire wafer, the C concentration increases with the number of defects in the films, but the increase is very small. It is not clear why the sapphire sample has the least amount of C. This is especially troubling given that Hashimoto et al. (*24*), determined that the GaN film they grew on the GaN template grown on a sapphire wafer contained 2 x 10^{17} cm^{-3} of C, whereas the sample film grown on the HVPE GaN substrate had only 1 x 10^{16} cm^{-3}. They attributed this to the larger number of dislocations in the former gettering more C. Later this same group fabricated SDs on GaN films grown by MOCVD on HVPE GaN substrates that had V_B = 1100 V (*1*). One possible reason for their lower C concentration obtained using an HVPE GaN substrate is that they grew their films at 1050 °C, whereas we grew ours at 1000 °C to keep the carrier concentration lower. It has been shown that less C incorporates in films grown at higher T (*25*), as well as higher pressure (*26, 27*) and V/III (*25*) ratio. We do not know at what pressure Saitoh et al. (*1*) grew their films, but it is virtually impossible to grow films by MOCVD at pressures that are greater than atmospheric. We do know that our V/III ratio of 3500 was greater than theirs, which was 2500. The SIMS data also

shows that the O impurity concentration varies only between 3 and 4 x 10^{16} cm^{-3} with the film on the sapphire substrate having the most O. There was substantially more O in the Ammono sample near the interface with the substrate, but it tailed off quickly as growth progressed. These values are close to that of Hashimoto et al. (*24*), which were a little higher with more being found in the GaN film grown on the GaN substrate. The measured Si concentration in our samples was also similar as it varied only from 4.2 – 5.5 x 10^{16} cm^{-3}; Hashimoto et al. (*24*) did not measure the Si content in their films. As noted earlier, all of the films were n-type. However, for the L- and H-HVPE samples the C concentration exceeded the Si and O doping concentration, suggesting that the material should be insulating if all of the Si and O atoms are donors, and the C is a deep acceptor. It is possible that there are N vacancies acting as donors (*8*), but it is also possible that not all of the C occupies N sites, or that all N sites are the same. Some of the C could be occupying Ga sites (*6*) or are interstials (*7*). Also, Elsner et al. (*28*) have shown through modeling that C is more tightly bound to the dangling bonds of dislocations than they are to the bonds in the bulk. This different interaction could alter the electrical properties. The C bound up in dislocations could also cause premature breakdown and could account for the wide variation in V_B across the wafer seen by us, as well as others (*29*). It is difficult, however, to accommodate this explanation with the wide variation of V_B seen in the Ammono samples, which have very few dislocations. Figure 12 shows the *n* vs φ curve for SDs on low doped HVPE wafer.

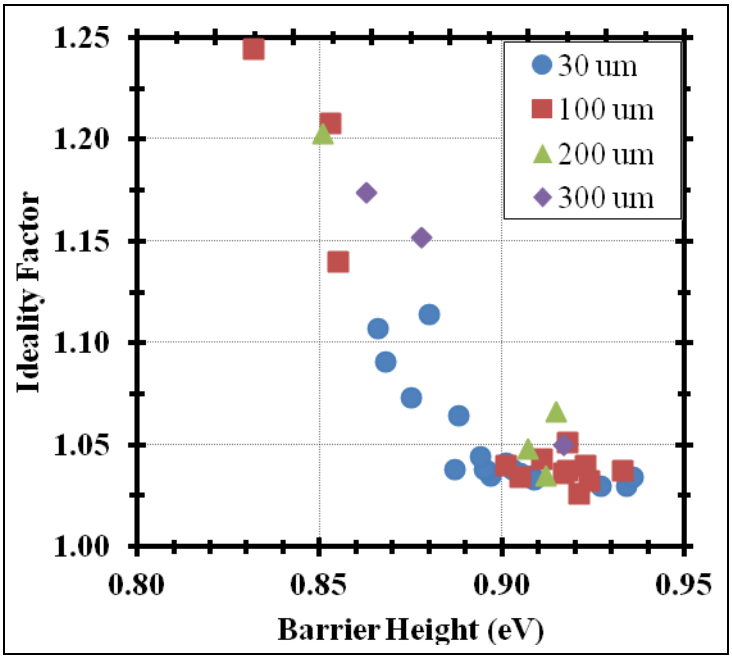

Figure 12. *n* vs φ curve for SDs on low doped HVPE wafer.

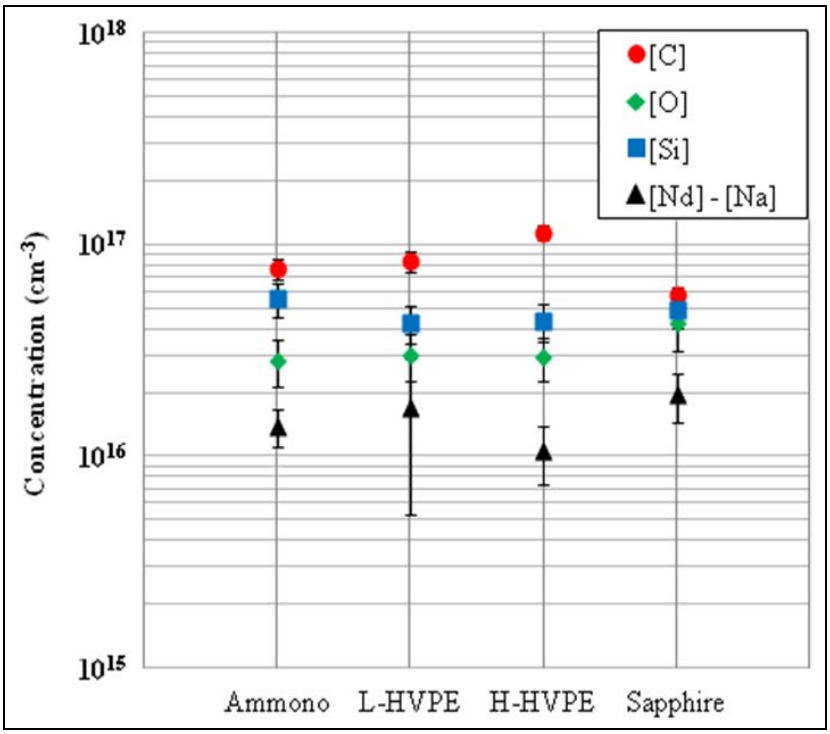

Figure 13. The C, O, and Si concentration measured by SIMS in the four wafers, and the net carrier concentrations determined by C-V measurements.

That the point defects in the MOCVD grown films play a detrimental role in the SDs is given more credence by the fact that the V_B for the front-side diodes fabricated directly onto an HVPE substrate doped 4.4 x 10^{15} cm^{-3} shown in figure 14 are much larger than any of those fabricated on the MOCVD grown films. V_B was as large as 803 V. The lower doping level can account for some of the increase in V_B, but it can account for only about half of the increase. The other half could be due to fewer point defects likely to be associated with C. The amount of C in the HVPE substrates is below the SIMS detectable limit of ~10^{16} cm^{-3}. As shown in figure 2, this is due to the fact that the Ga source is gallium chloride (GaCl), as opposed to $(CH_3)_3Ga$.

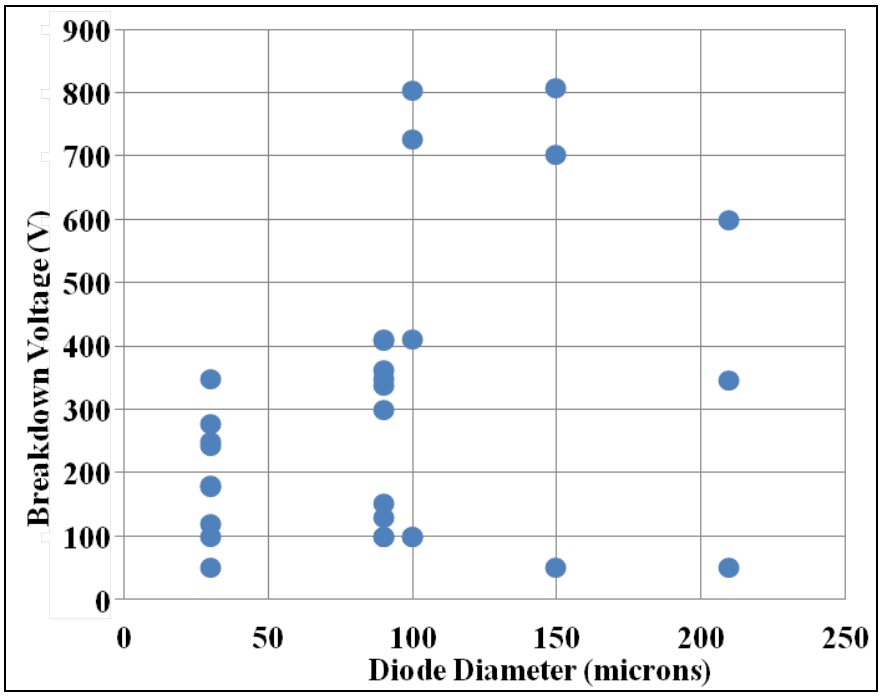

Figure 14. V_B plotted as a function of the diode diameter for front side diodes fabricated on an HVPE wafer doped 4.4 x 10^{15} cm^{-3}.

3.3 Substrate Resistance

The median $R_{ON \cdot SP}$ for the four samples with MOCVD films grown on the different substrates displayed in figure 15 show that the diodes fabricated on the L-HVPE substrates have by far the largest values. This is expected because the L-HVPE substrate is resistive, and the resistance is much larger than that of the low doped film because it is almost 100 times thicker. At the other extreme $R_{ON \cdot SP}$ is much smaller for the films grown on the Ammono substrate because they are doped in the high 10^{18} cm^{-3} so that its resistance is much less than that of the film making its contribution to the total resistance insignificant. The H-HVPE substrate doped in the low 10^{18} cm^{-3} lies in between with a substrate resistance a little larger than that of the film because the electron mobility in the more highly doped substrate is smaller.

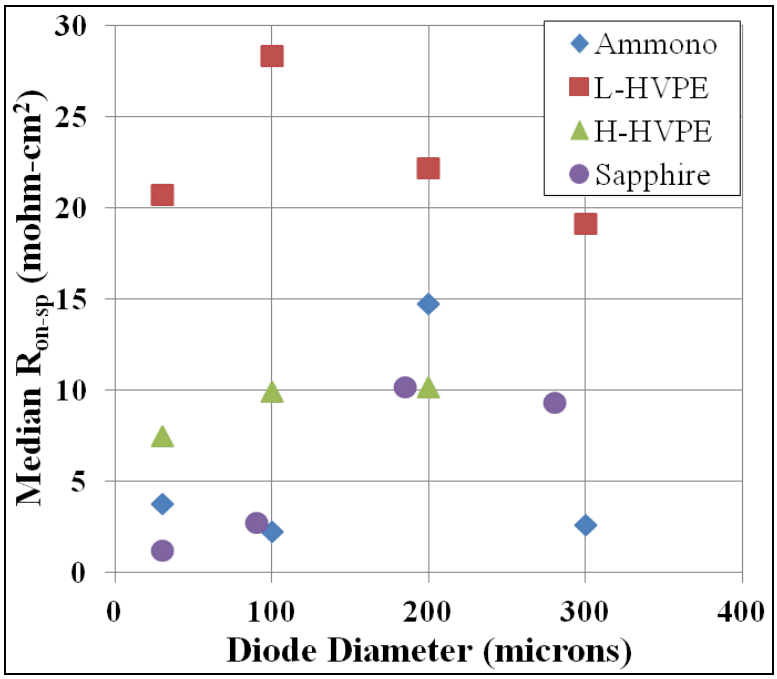

Figure 15. Median $R_{ON\cdot SP}$ for the four different substrates with MOCVD films grown on them.

$R_{ON\cdot SP}$ is relatively small for the films grown on the sapphire substrate because the current does not have to pass through the substrate. The more critical issue is that the template must contain an n^+ layer beneath the active low doped film on which low contact resistance ohmic contacts can be fabricated. Also, care must be taken not to ion beam damage the region where the contact is made during the etching process. The front-side diodes we fabricated directly on a low doped HVPE substrate had larger $R_{ON\cdot SP}$ than those fabricated on the film grown on the sapphire substrate because the contact resistance was higher. The HVPE substrate did not have an n^+ layer grown on it, and there was evidence that the reactive ion etching process left some damage in the region where the contacts were made. This problem can readily be overcome, as is evidenced by the work of Saitoh et al. (*1*), whose record setting SDs with front side contacts had $R_{SP\cdot ON} = 0.71$ mΩ/cm^2. It is highly likely that they grew an n^+ GaN film on their HVPE substrate before they grew the low doped film, and that they etched away the etch damage prior to forming the ohmic contacts.

The experimental evidence discussed previously strongly suggests that we should attempt to grow low doped HVPE films. This would enable us to eliminate the problem associated with C contamination from MOCVD grown films, and it would also enable us to use a high doped HVPE and/or an Ammono substrate. Prior to the development of the MOCVD process, all of the III-V films such as GaAs were grown by the chloride or hydride technique both of which use GaCl as the source of the Ga, and C concentrations are believed to be in the low 10^{14} cm^{-3} range as determined by photoluminescence. The primary reason the MOCVD method is now used to grow most III-V films is because the flow of the gaseous constitutions can be more closely

controlled. This enables one to grow device structures that require atomic layer accuracy such as those that require quantum well structures. The primary impurities will likely be Si and O produced by the reaction of the hydrogen chloride (HCl) gas with the quartz reactor, and the problem will likely be more severe for GaN than it was for GaAs because GaN is grown at a higher temperature.

Besides trying to keep the background impurity concentration below 10^{16} cm^{-3}, it will also be a challenge to grow a film with good structural quality even when a high quality GaN substrate is used. Hydride films grow very fast because the deposition process is very efficient. The reactants, GaCl and NH_3, are readily "grabbed" by the substrate surface making it a challenge to create conditions where the atoms can find their equilibrium positions. As a result small angle grain boundaries can form easily. This, in fact, is what happened with our one attempt to grow an HVPE film on the HVPE substrate, as shown in figure 16 where one of the asymmetric RCs is displayed. One can see that the broad peak, that is 1578″ wide, is composed of a number of peaks from almost identically oriented grains. With peak widths of ~150″ the symmetric peaks were reasonably narrow. This shows that the small angle grain boundaries are created by slight rotations about the *c*-axis.

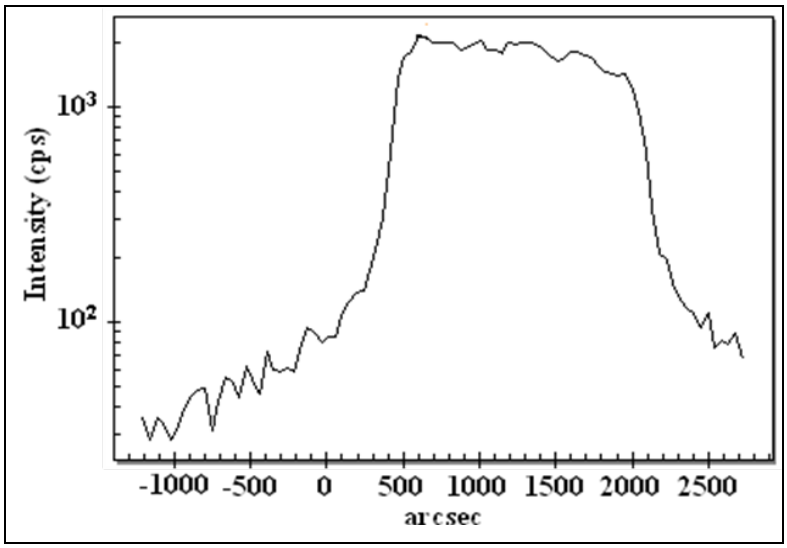

Figure 16. Asymmetric rocking curve for an HVPE film grown on an HVPE substrate.

Although challenging, this is not an insurmountable problem. For other III-V compounds it was solved by using substrates that were slightly misoriented from the axis by a degree or two. The substrate we used was directly on-axis. We were hindered from pursuing this further because the material was being grown on an SBIR program by Kyma Technologies. Their Phase II proposal was awarded in January 2011, but funds could not be put on it because DCAA did not approve of Kyma's accounting system. It took until a week ago—almost one year later—for Kyma to get its accounting system approved. Hopefully we will begin to renew this work in January 2012.

4. Future Work

The next steps are to improve the SDs by learning how to grow high doped, high quality substrates and low doped, high quality films by HVPE; apply what we learn about the SDs to the gate of a high power HEMT, and to explore the possibility of learning how to fabricate high quality AlGaN device structures on GaN or aluminum nitride (AlN) substrates.

4.1 High Doped Substrates and Low Doped Films

The substrates should be doped $>10^{18}$ cm^{-3} and have a resistivity of 10^{-2}–10^{-3} Ω·cm, which translates into a specific resistance of 0.35–0.035 mΩ·cm^2 for 350 µm thick wafers. The likely dopant will be Si. It has been noted when growing thick films that defects are more readily created in Si-doped films, but when great care is taken, the difference in the quality of the doped and undoped films is slight. Learning how to do this will be one of Kyma's prime objectives in their Phase II SBIR; being able to demonstrate they can grow GaN substrates that can produce SDs with a large FOM will help their business.

4.2 HPE HEMTs

Low doped HVPE films will also be grown by Kyma. They believe if they can find the correct off-cut, they will be able to grow films with a defect structure comparable to the substrate they grow it on. They will also experiment with growing relatively thin AlGaN films by HVPE that are required for HEMTs. It might not be so critical to reduce the C concentration in these films, although it has been suggested that C impurities contribute to the gate leakage. We anticipate that our relationship with SUNY-Albany will continue for another year, and both we and they will be growing HEMT structures by MOCVD, but they will be growing their structures on Si, as displayed in figure 17. The driving force for growing the material on Si is that Si substrates are inexpensive and this would enable multi-functional processing of information. However, the lattice mismatch is very large, so the challenges will be large also.

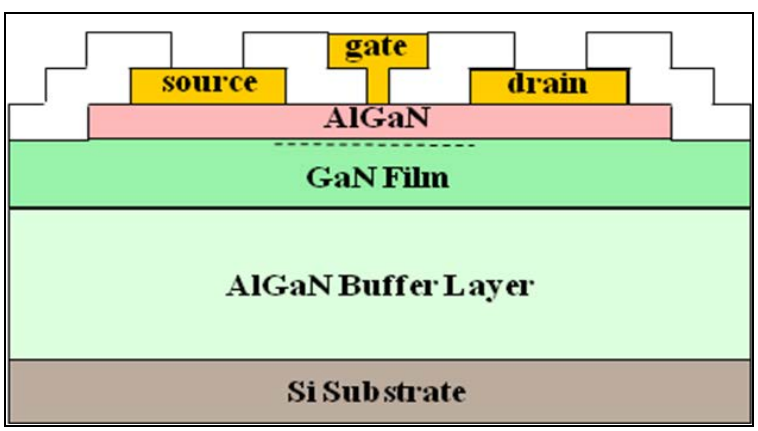

Figure 17. Schematic of a GaN/AlGaN HEMT structure grown on Si.

4.3 Modeling AlGaN Film Growth on AlN and GaN Substrates.

In the long term we would like to be able to grow AlGaN on high quality GaN or AlN substrates in such a way that the dislocations are confined to the region of the interface, and only a few propagate up to the AlGaN surface where the devices are fabricated and/or the high electrical stress points occur. This would enable us to grow AlGaN of any composition with low concentrations of dislocations for any aluminum content. It has already been achieved in silicon germanium (SiGe) film growth on Si substrates by grading the SiGe layer or growing superlattice steps with an increasing Ge concentration (*30*). This work is being pursued under a director's research initiative (DRI); one of the outcomes is that we have identified the (11$\underline{2}$2) plane, shown in figure 18, as the probable pyramidal slip plane in the hexagonal wurtzite structure of GaN when growth is done on the basal (0001) plane. We hope we will be able to transfer this effort to the multi-scale modeling program of electronic materials and continue to couple it with this DSI program. An STTR on this subject has also been submitted by ARO.

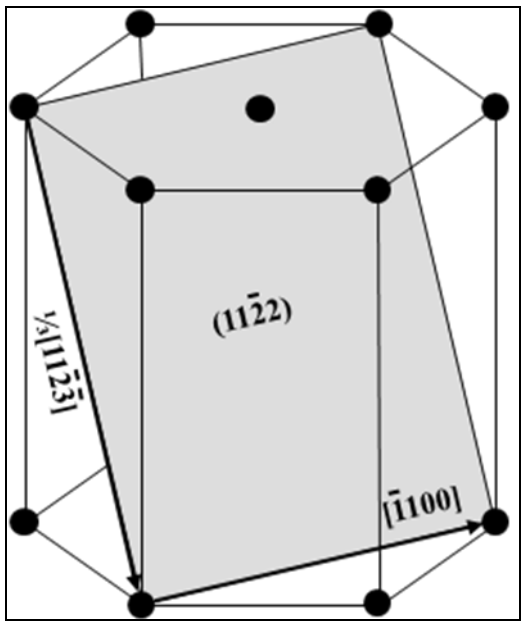

Figure 18. Schematic of the wurtzite (11$\underline{2}$2) pyramidal slip plane.

The driving force for this work is that AlN has significantly better parameters than either GaN or SiC for high power applications. Because its E_G = 6.2 eV is almost twice that of the other two, its ξ_C = 11.7 MV/cm (*31*) is much larger. This is offset to some extent by its smaller electron mobility, thought to be 426 $cm^2/V\cdot s$ (*32*), but it still has a much higher FOM, as shown in figure 19, because the FOM α V_B^2. There is some concern that the Si donor level is too deep, but it has recently been determined to have a depth of only 65–75 meV (*33*), which is significantly smaller than the depth of the magnesium (Mg) acceptor in GaN, which is ~120 meV. Also, high quality AlN crystals are already being grown because it is actually easier to grow them than GaN crystals, due to the fact that the N vapor pressure is much less than it is for GaN—the Al-N bond is much stronger. Most likely there will be compromises and AlGaN will be used. AlGaN is not

lattice matched to either GaN or AlN crystals, so it is essential that we learn how to grow AlGaN on AlN or GaN like they do SiGe on Si, be it by graded junction or a stepped superlattice (*30*).

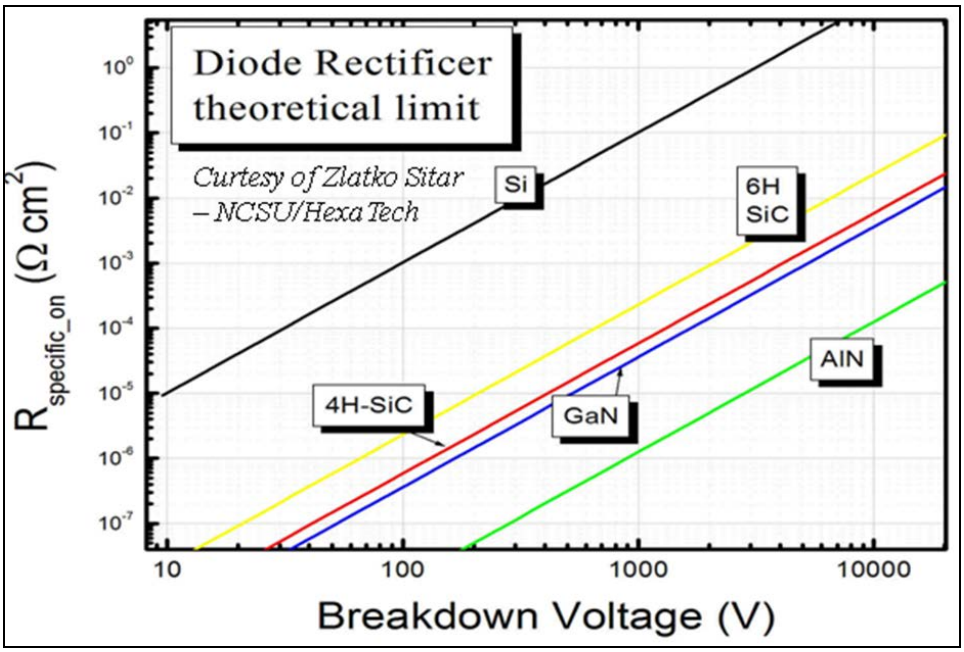

Figure 19. Plot of the ideal breakdown voltage as a function of the specific on resistance for AlN, as well as for Si, SiC and GaN.

5. Conclusions

Great strides have been made in the fabrication and understanding of the operation of SDs. We achieved our goal of routinely making diodes with $V_B > 600$ V, which is the first plateau for HPE diodes, e.g. it is the buss voltage for DC → AC inverters in electrical vehicles. The largest value we obtained was $V_B = 897$ V. Although we have not yet matched the record setting work by researchers in Japan working over a number of years (*1*), we expect to soon be able to meet or exceed their values of $V_B = 1100$ V and FOM = 1.7 GW/cm^2, which is better than the best achieved for SiC and even exceeds its theoretical value, because we now understand what the important factors are.

One important factor is that carbon, most likely coming from the decomposition of $(CH_3)_3Ga$ at the high growth temperature of MOCVD-grown GaN films, creates point defect traps that cause premature breakdown in the SDs. Although these effects can to some extent be mitigated by growing the films at higher pressures and temperatures, they continue to be an important factor. We now believe that the films should be grown by HVPE because the reactants do not contain C. We recognize that keeping the background Si and O impurities low will be a challenge because the HCl used in the HVPE process could attack the quartz reactor and create vapor phase Si

and/or O containing species. Through Kyma, we made one attempt to grow HVPE films and we achieved some limited success, but we were not able to continue this work because the Phase II effort where this would have been done was not given the funding for almost a year because DCAA took almost a year to approve Kyma's accounting system, and the funding still has not been released.

Not having Kyma to work with also stymied our efforts to obtain and test SDs fabricated on a more conducting HVPE substrate to reduce $R_{SP \cdot ON}$ and increase the FOM. This will be the second primary topic that Kyma will focus on when the Phase II SBIR funds are finally released.

We did determine that dislocations did not play as important a role in the premature breakdown of SDs as was originally thought. This discovery was made by simultaneously growing device structures on substrates with increasingly more dislocations. These substrates were an ammono-thermal solution grown substrate with ~5 x 10^3, an HVPE substrate with ~5 x 10^6, a doped HVPE substrate with ~5 x 10^7, and a GaN template grown on sapphire with ~5 x 10^9 dislocations cm^{-2}. Surprisingly, V_B for the SDs fabricated on the ammono-thermal substrate were much less than those for the SDs fabricated on the better HVPE substrate. It appears that, although dislocations play an important role, the problems created by the background C dominate them. We will test this hypothesis once Kyma comes on line with its Phase II funding. This will be done by fabricating and testing HEMTs, as well as SDs.

Looking to the future, we also determined through modeling with DRI support that the likely slip plane for the mismatch dislocations created during the growth of (0001) oriented AlGaN on GaN or AlN substrates is the $(11\underline{2}2)$ plane. This could be the first step towards learning how to grow low dislocation AlGaN films much like low dislocation SiGe films can be grown on Si substrates. The reason this is important for high power electronics is that AlGaN should have an even larger breakdown field than SiC or GaN, which might enable us to make devices for some pulsed power applications that currently cannot be achieved. We hope this work will be continued theoretically under the multi-scale modeling program for electronic materials and experimentally under a proposed STTR with ARO.

6. References

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List of Symbols, Abbreviations, and Acronyms

2DEG	two-dimensional electron gas
AlGaN	aluminum gallium nitride
ARO	Army Research Office
C	capacitance
C-V	capacitance-voltage
DCAA	Defense Contract Audit Agency
DRI	Director's research initiative
ECCI	electron channeling contrast imaging
E_G	energy gap
GaN	gallium nitride
FOM	figure of merit
HEMT	high electron mobility transistor
H-HVPE	high doped HVPE
HPE	high power electronics
HVPE	hydride vapor phase epitaxy
ICP	inductively coupled plasma
I-V	current-voltage
L-HVPE	low doped HVPE
MBE	molecular beam epitaxy
MOCVD	metal-organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field effect transistor
n	semiconductor ideality factor
RF	radio frequency
RFOM	relative figure of merit

$R_{ON \cdot SP}$	specific on-resistance
SBIR	Small Business Innovative Research
SD	Schottky diode
SiC	silicon carbide
SIMS	secondary ion mass spectroscopy
STTR	SBIR and Technology Transfer Research
T	temperature
TMGa	trimethyl gallium
UID	unintentionally doped
UV	ultraviolet
V	voltage
V_B	breakdown voltage
W_B	depletion layer width at breakdown
ξ_C	critical electric field
ε	electric permittivity

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