



U.S. ARMY  
**RDECOM**

Energy Efficient Software Improvements for  
Constrained Devices



## S&T Campaign: Computational Sciences Computing Sciences

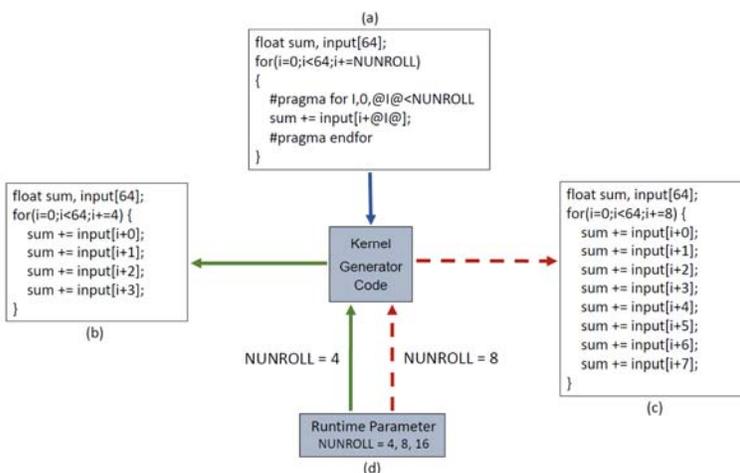
Song Jun Park, (410) 278-5444  
song.j.park.civ@mail.mil

### Research Objective

- Design effective programming methodologies for energy efficient architectures
- Attain high performance without sacrificing productivity

```
#pragma for I, 0, NPARTICLES-1
T4 p@I@ = pbuf[NPARTICLES*get_global_id(0) + @I@];
T4 a@I@ = (T4)(0.0, 0.0, 0.0, 0.0);
#pragma endfor
for(uint i = 0; i < n; i += NUNROLL) {
    T4 p, dp;
    T i nvr;
    #pragma for J, 0, NUNROLL-1
    p = pbuf[i+@J@];
    #pragma for I, 0, NPARTICLES-1
    dp = p - p@I@;
    i nvr = rsqrt(FMA(dp.x, dp.x, FMA(dp.y, dp.y,
        FMA(dp.z, dp.z, eps))));
    a@I@ = FMA(p.w, i nvr*i nvr*i nvr*dp, a@I@);
    #pragma endfor
    #pragma endfor
}
```

Code snippet depicting the auto-tuning technique for kernel parameterization.



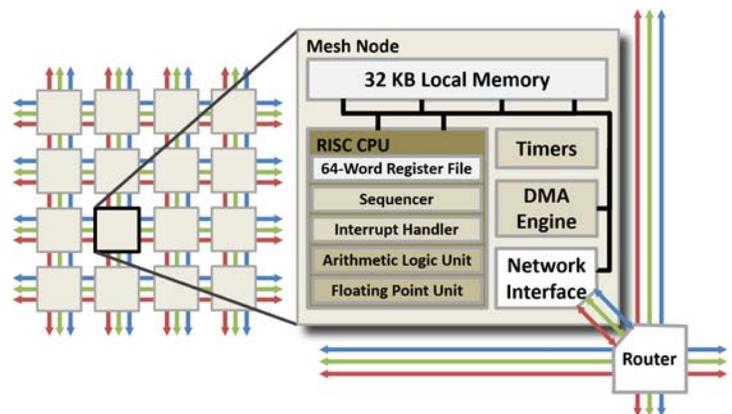
Pre-processor code generation scheme. For example, @I@ is replaced with loop index inside '#pragma for' statements.

### Challenges

- The breakdown of Dennard scaling and the rise of dark silicon
- How to advance computing systems without advance in processing technology
- Ninja gap of 24X

### ARL Facilities and Capabilities Available to Support Collaborative Research

- Adaptive's Epiphany architecture Parallalla boards
- ARM platforms
- Publications
  - Richie, Ross, Park, and Shires, "Threaded MPI Programming Model for the Epiphany RISC Array Processor," *International Conference on Computational Science (ICCS)*, 2015
  - Ross, Richie, Park, and Shires, "Parallel Programming Model for the Epiphany Many-Core Coprocessor Using Threaded MPI," *Proceedings of the 3rd International Workshop on Many-core Embedded Systems (MES)*, 2015
  - Ross, Richie, and Park, "Implementing Image Processing Algorithms for the Epiphany Many-Core Coprocessor with Threaded MPI," *IEEE High Performance Extreme Computing (HPEC)*, 2015
- Achieved high performance for the Epiphany architecture with efficient parallel programming model, threaded MPI



Epiphany MIMD architecture is a scalable array of RISC cores connected in a 2D mesh network.

### Complementary Expertise/ Facilities/ Capabilities Sought in Collaboration

- Approximate computing
- Reconfigurable computing (Arria 10)
- Tile architectures (Tilera, Kalray, etc)
- Power architectures
- Domain specific accelerators