

Energy Efficient Electronics



S&T Campaign: Materials Research Electronics

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Research Objective

- 10x reduction of the electronic load of the Soldier /Squad level communication equipment by attacking key challenges at the material, device, circuit, and subsystem levels



ARL Facilities and Capabilities Available to Support Collaborative Research

- Extensive test and characterization facilities spanning digital, analog and mixed signal; frequencies up to 220GHz.
- Complete custom ASIC design environment including full Cadence suite
- 2.5 (MoM) and 3D EM solvers for both circuit and structure design
- Wafer/die level probe stations with instrumentation up to 110 GHz
- Internal wirebonding & QFN packaging capability

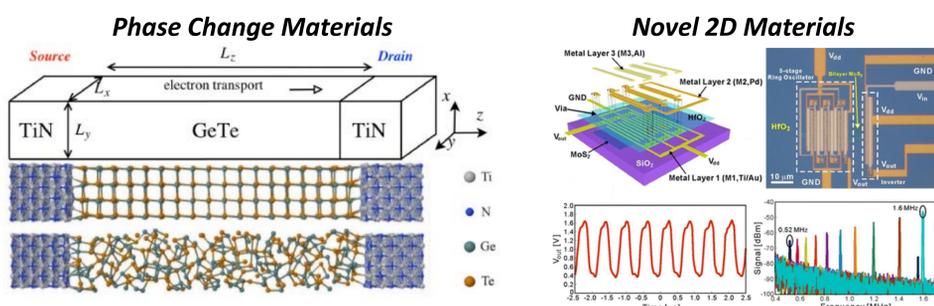
Ultimate Transmission Balasubramanian, S. ; Boumaiza, S. ; Sarbishaei, Hassan ; Quach, T. ; Orlando, P. ; Volakis, J. ; Creech, G.; Wilson, J. ; Khalil, W. Microwave Magazine, IEEE Volume: 13 , Issue: 1 DOI: 10.1109/MMM.2011.2173983 Publication Year: 2012 , Page(s): 64 – 82 Cited by: Papers (10)

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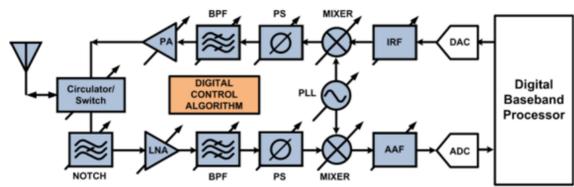
Nano-electromechanical storage element for a low power complimentary logic architecture using PZT relays Proie, R.M. ; Polcawich, R.G. ; Pulskamp, J.S. ; Ivanov, T. ; Zaghoul, M. Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International DOI: 10.1109/TRANSDUCERS.2011.5969633 Publication Year: 2011 , Page(s): 840 - 843

Challenges

- End of Moore's Law signifies the end of "easy" power scaling
- Military communication requires extremes across all domains – temperature and RF environment, lifetime of operation – that limit use of commercial solutions
- Requires comprehensive solution spanning materials through the waveform



Reconfigurable and Adaptive Front Ends

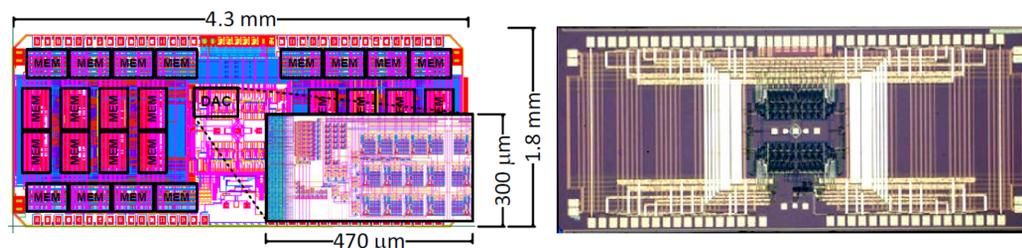


Efficient Waveforms



Complementary Expertise/ Facilities/ Capabilities Sought in Collaboration

- Advanced packaging (3D integration or System-in-Package)
- Collaborate with ARL on design and concepts for low power draw RF front ends and sensors
- VLSI & integrated electro-optic design tools



- InP-CMOS DAC
- 32Gbps, 8-bit
- ARL design under DARPA COSMOS