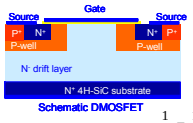
SiC MOS Device Physics in Support of Power Device Development

Aivars Lelis, Dan Habersat, Ron Green, and Tsvetanka Zheleva
Sensors and Electron Devices Directorate,
Energy and Power Division,
Power Components Branch (RDRL-SED-E)

Objective:

Develop more reliable, high-performance SiC power MOSFET switches to meet advanced Army requirements

- High blocking voltage in OFF-state with low drain leakage
- Low ON-state resistance
- Low switching losses
- High-temperature operation
- Long-term reliability



Schematic DMOSFET

➢Charge Trapping at/near SiC/SiO$_2$ interface

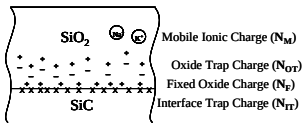
➢Surface Roughness

$$\frac{1}{\mu_{Ch}} = \frac{1}{\mu_B} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}$$

Tech. Challenges:

Identify, understand, and reduce process and stress-induced material defects

- Causes increased charge trapping and surface roughness
- Decreases μ_{CH} and increases ΔV_T

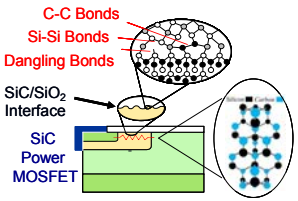


➢Develop proper reliability test methods
➢Develop predictive methods
➢Develop process and design improvements

Approach:

In-house and collaborative

- Materials analysis
- Electrical characterization
- Device modeling



Interfacial Charge

Key Advantages:

SiC is a wide bandgap semiconductor

- Low n_i => high-temperature operation
  => reduced cooling requirement
  => less wt. and vol.
- Large critical field => high-voltage operation w/ lower R_{ON}
- Large therm. cond. => reduced ΔT due to self-heating
- Large $v_{sat.}$ => high-frequency operation
  => reduced size of passives
  => less wt. and vol.

SiC MOSFETs:

- HT Replacement for Si IGBTs for Power Conversion
  - Large reduction in conduction and switching losses
- Voltage-controlled, Normally Off (vs BJT or JFET)
- Improved power management and energy efficiency
  - Motor drives and hybrid-electric vehicles

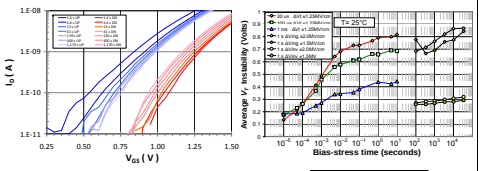
Summary of Impact:

- **Identified HTRB and TDDB reliability issues**
  - Feedback to device manufacturer has led to improved device processing and test methods
- **Identified V_T instability reliability issue**
  - Increases drain leakage and R_{ON} — worse at HT
  - Tunneling to oxide traps incorporated into comprehensive physics-based device model
  - Identified E-prime center as main oxide trap
- **Identified transition layer degradation in SiC**
  - Correlated TL thickness, μ_{CH}, and interface traps
  - Identified Si vacancy in SiC as main interface trap

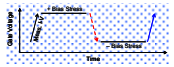
In-house work:

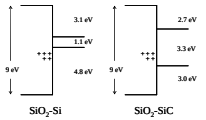
V_T Instability:

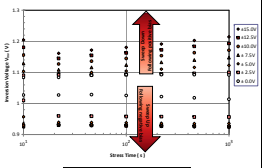
- **Key experimental results**
  - Positive shift in I-V char. due to positive bias stress and negative shift in I-V char. due to negative bias stress
  - Effect is repeatable
  - Linear increase in ΔV_T w/ log stress time
  - Polarity-dependent sensitivity to bias stress magnitude
  - Increase in ΔV_T w/ decrease in measurement time: (Fast and Slow I-V)
  - Subthreshold slope dependence on measurement sweep direction
  - Observation of V_{FB} instability in MOS capacitors
  - Significant increase in ΔV_T w/ increasing T and superlinear increase w/ increasing stress time
  - Increase in ΔV_T w/ ON-state current stress



$$\Delta V_{OT} = \frac{q \cdot \Delta N_{OT}}{C_{ox}} \approx \Delta S \cdot \frac{\beta \cdot \Delta W_A}{\ln(10)}$$



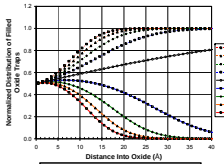


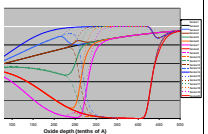


$$\beta = \sqrt{\frac{m_e^*}{\hbar^2} \cdot (E_i - q \cdot \mathcal{E}_{ox} \cdot x_m)}$$

Tunneling Modeling:

- **Tunneling rate reflects trap dist.**
  - Linear w/ log(t) for flat distribution
  - 2-Å/dec rate for Si => 40-Å deep
- **Two-way tunneling model**
  - Balance btwn e$^-$ tunneling in & out
  - Explains meas. time dependence and bias-stress mag. dependence
  - Possible two-step process for e$^-$ tunneling in from interface traps





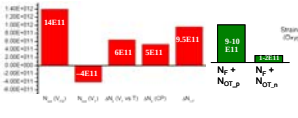
$$n_{OT}(x,t=\infty) = \frac{1}{1 + \left(\frac{\alpha_r}{\alpha_a}\right) \cdot \exp(-2 \cdot (\beta_a - \beta_r) \cdot x_m)}$$

$$p_{non_e} = \alpha \cdot \exp(-2 \cdot \beta_a \cdot x_m)$$

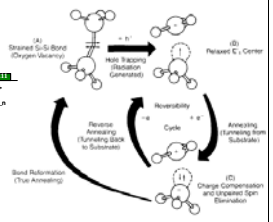
$$\Delta n_{OT}(x,t) = \Delta t \cdot [p_n \cdot (n_{dist} - n_{OT}(x,t)) - p_e \cdot n_{OT}(x,t)]$$

Defect Analysis:

- **Charge separation results**
  - Identification of E-prime centers as oxide trap: oxide traps are either pos. charged or neutral
  - $N_F + N_{OT}$ results under pos. and neg. bias stress suggest N_F not significant—focus on reducing N_{OT}
- **High-temperature bias results**
  - Si NBTI results: E-prime center defects increase dramatically at elevated temp., but only under bias
  - Identification of E-prime centers as oxide trap: explanation of large increase in V_T instability at high temperature

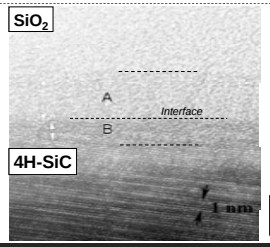


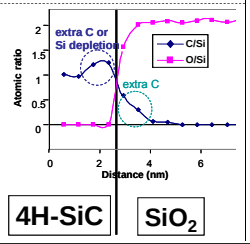
$$N_{Inet} - N_{IT_\{CP \text{ or } \Delta Nnet(T)\}} = N_F + N_{OT}$$
$$\Delta N_{OT} = (N_F + N_{OT_p}) - (N_F + N_{OT_n})$$



SiC Transition Layer:

- **Transmission Electron Microscopy (TEM) results**
  - First to show existence of transition layer (TL)
  - Thermal oxidation process involves structural degradation (to amorphization)
- **Electron Energy Loss Spectroscopy (EELS) results**
  - Indication of formation of a ternary SiOxCy phase in the vicinity of the SiC/SiO$_2$ interface
  - Excess carbon on both sides of the interface
- **Correlation observed between TL thickness and μ_{CH}**





Collaborations:

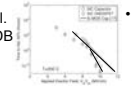
CREE and GE (*Large-area power MOSFET Development*)

- Large area DMOSFETs
- Power converter module demo

67A DMOSFET
8 mm x 7 mm
0.406 cm^2

National Inst. of Standards and Technology (*Electrical Char.*)

- Gate oxide rel. studies—TDDB
- Fast I-V

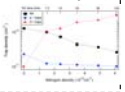


RPI (*Electrical Char.*)

- Hall mobility

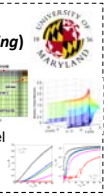
Auburn, Rutgers (Vanderbilt), and Purdue (*Device Processing and Materials Analysis*)

- Gate oxidation optimization to reduce N_{IT}, N_{OT}, and N_F
- MEO investigation
- Physical effect of N (and P)



University of Maryland (*Physics-based Device Modeling*)

- Power MOSFET—ON and OFF state vs temperature
- Transient analysis during switching; current sharing
- Incorporation of tunneling model
- Mobility—effect of TL and surface roughness; Hall meas.

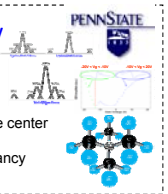


University of MD (& Univ. of TN Knoxville) (*Materials Analysis*)

- TEM, EELS analysis of SiC TL
- Si-O-C phase analysis
- Correlation of N anneal, TL thickness, and μ_{CH}

Penn State University (*Materials Analysis*)

- ESR, SDR, and SDT defect analysis
- Observation of E-prime center defect in oxide (N_{OT})
- Identification of Si vacancy defect in SiC (N_{IT})



Future Work:

- **Continue to Lead Technical Effort**
  - Support manufacturable device development and key university research
  - Host annual workshop of most U.S. experts from academia, industry, and government
- **Develop Improved Reliability Testing Methods**
  - Automotive industry test methods for Si power device evaluation need correction for SiC
  - Collaborate w/ device manufacturers to ensure proper reliability evaluations for HTRB, etc.
  - Collaborate w/ NIST to determine accurate expected lifetimes of fully processed devices
- **Continue Development of Comprehensive Physics-Based Device Simulator**
  - Collaborate w/ UMD in incorporating latest physical insight from materials analysis and electrical characterization—including Hall mobility measurements
  - Model transient effects during switching of power DMOSFETs
  - Improve device design to reduce impact of defects
- **Develop Improved Gate Oxide Processing Methods to Reduce V_T Shift**
  - Collaborate w/ Penn St to confirm E-prime center is major oxide defect using ESR, EDMR
  - Collaborate w/ Cree, GE, and Auburn to incorporate Si oxide processing methods appropriate for reducing E-prime defects—and better understand role of N during post-oxidation NO anneal
- **Develop Improved Gate Oxide Processing Methods to Improve μ_{CH}**
  - Collaborate w/ UMD and UTK, and device manufacturers to perform TEM, EELS, XPS to better understand relationship between oxidation conditions, SiC TL, and μ_{CH}
  - Collaborate w/ Auburn and Purdue to understand role of Metal-Enhanced-Oxidation (MEO) in improving mobility w/out decreasing N_{IT}
  - Collaborate w/ UMD and Cree to understand relationship between coulombic and surface-roughness scattering

POC: (301) 394-5426